BERKELEY LAB
Bringing Science Solutions to the World

U.S. DEPARTMENT OF ENERGY
Office of Science

Custom ICs for Physics Research

HEPCAT Summer School @ SLAC Seminar

Carl Grace 8/28/2024

Lawrence Berkeley National Laboratory

Lawrence Berkeley National Laboratory

MOST DIVERSE US NATIONAL LABORATORY

Key Strengths

Physical Sciences, Computing, Biosciences, Earth and Energy Sciences, Materials, and Nanotechnology

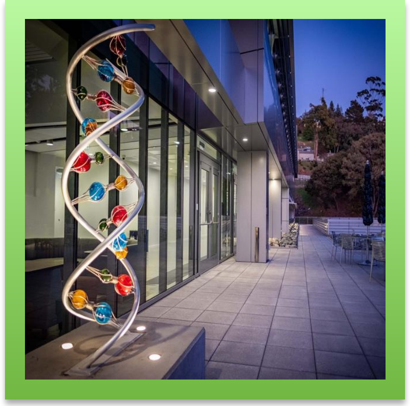
EXCELLENCE & DIVERSITY

3500 employees
1000 students

1750 visiting researchers

NATIONAL USER FACILITIES

- Advanced Light Source
- National Energy Research Scientific Computing Center
- Energy Sciences Network
- Joint Genome Institute
- Molecular Foundry (including National Center for Electron Microscopy)

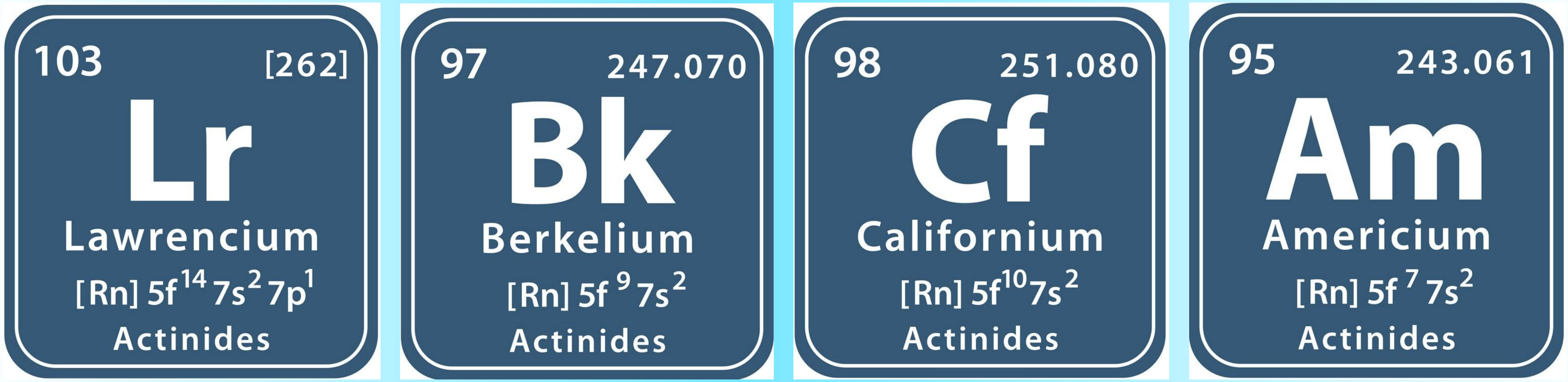


16 NOBEL PRIZES

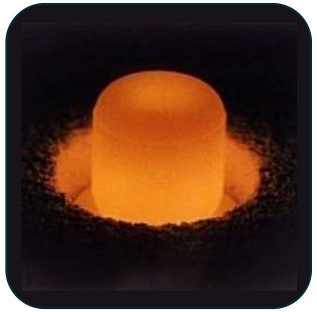
Most recent: 2020 Nobel Prize in Chemistry for co-discovery of CRISPR gene editing (Prof. Jennifer Doudna)

Fun Fact

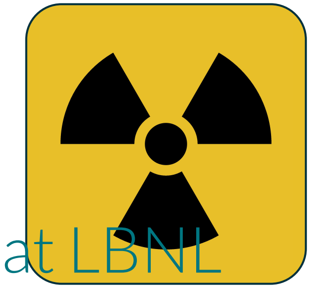
LBNL may be the only workplace where you can **write your address in elements!**



All discovered by LBNL along with 12 other elements!



Plutonium discovered in 1940 at LBNL



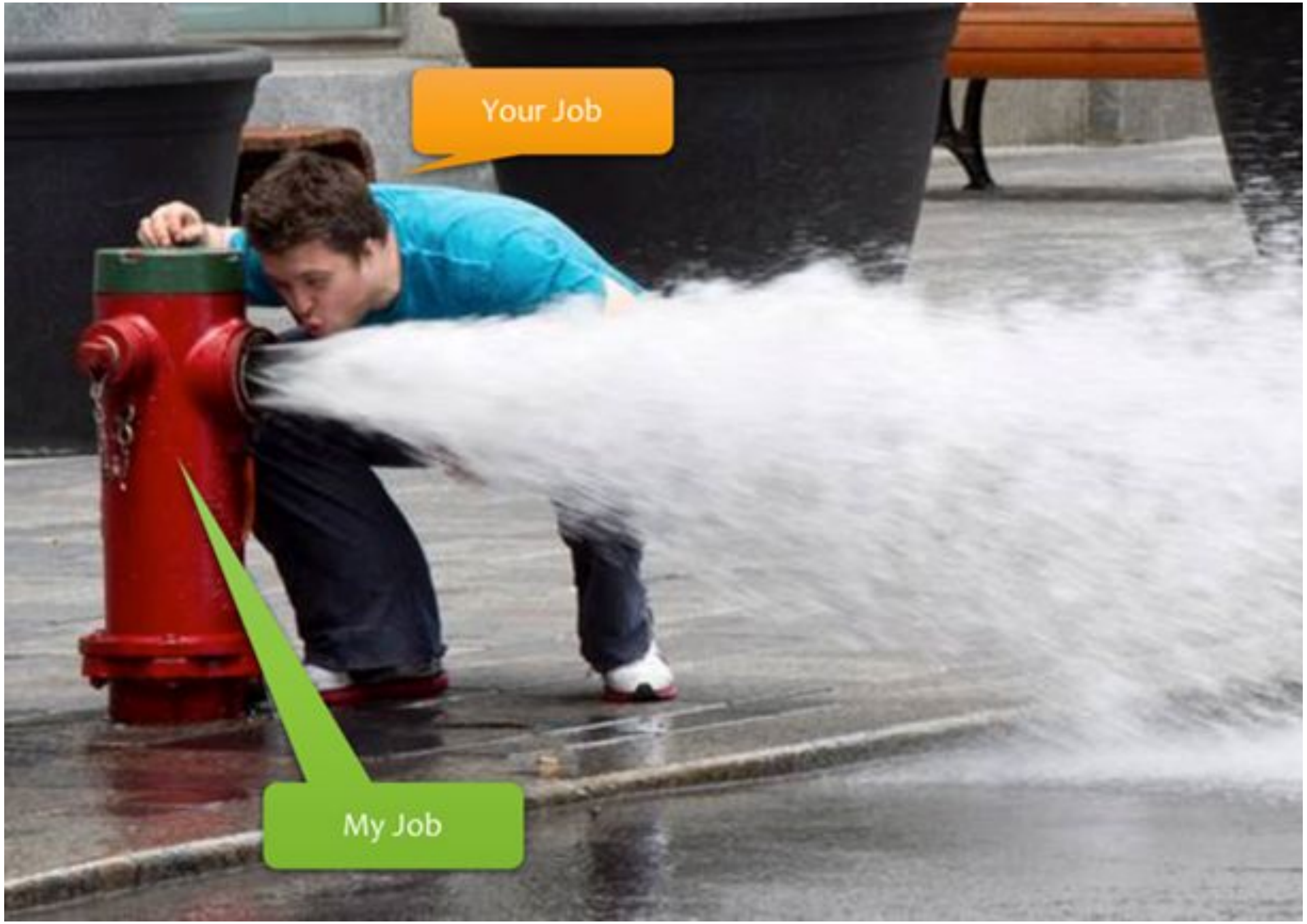
Radiation hazard trefoil invented in 1946 at LBNL

Introduction

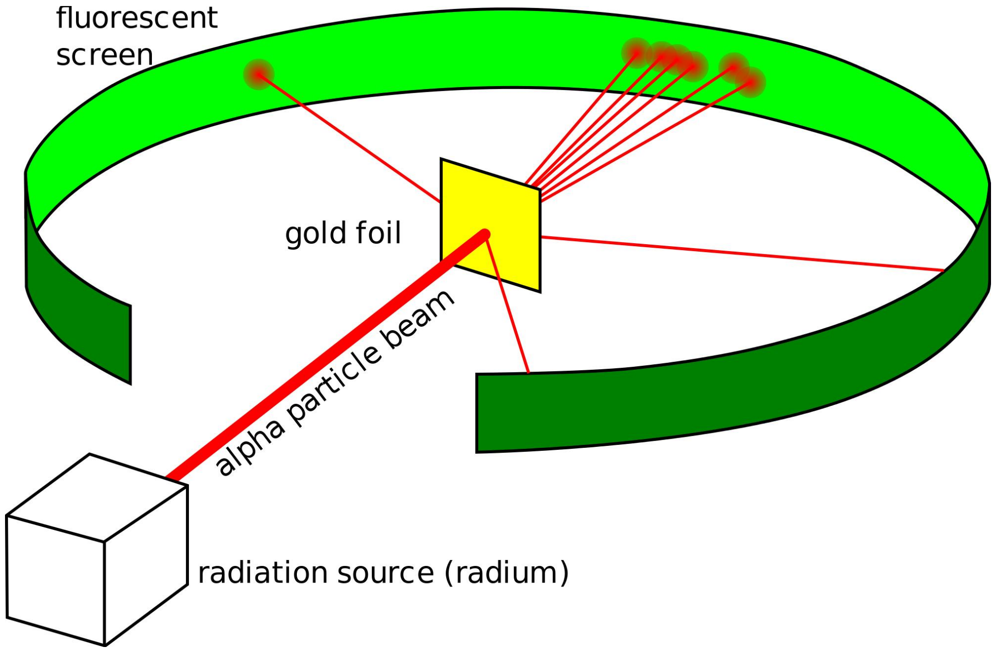
- Custom Integrated Circuits – also called Application-Specific Integrated Circuits (ASICs) - are an increasingly important technology for experimental physics

- ASICs are an enabling technology. Without ASICs, many modern detector systems would not be feasible

- The goal of an ASIC in HEP is to generate data that physicists can turn into papers



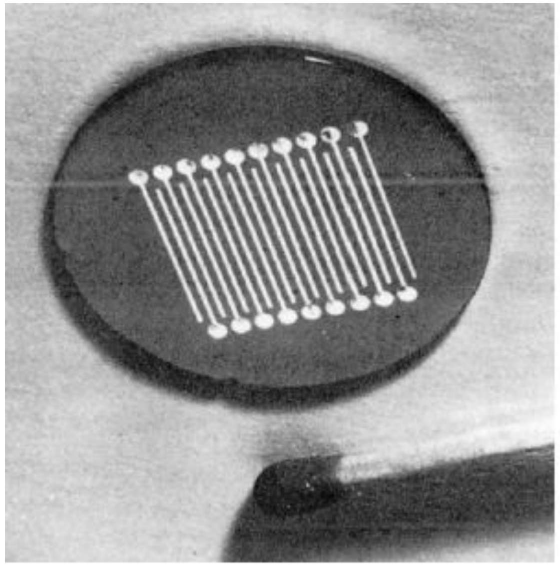
Detector Readout

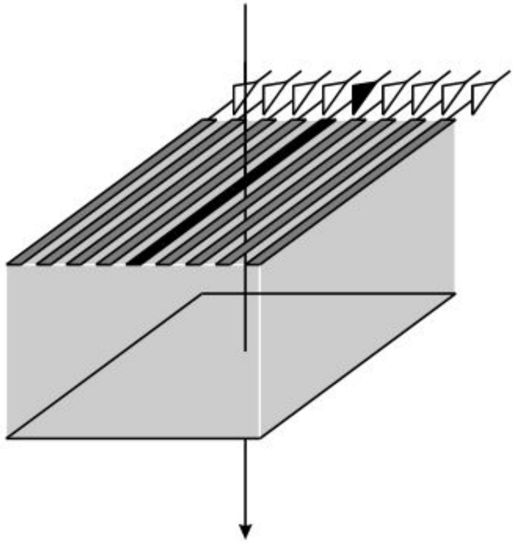


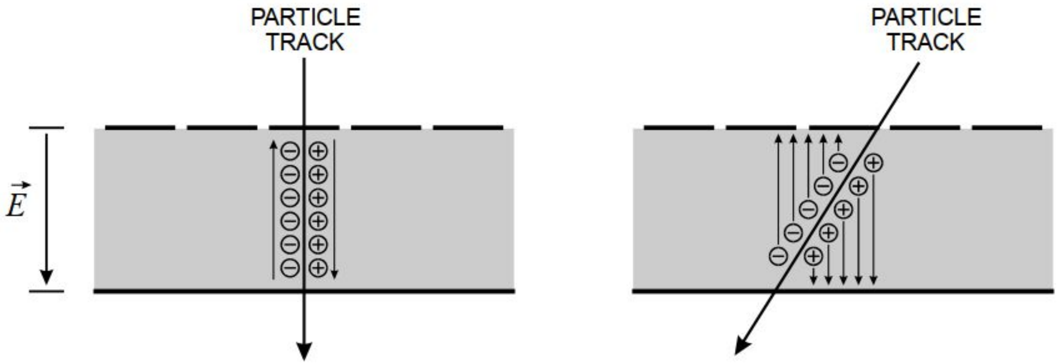
Rutherford's discovery of the atomic nucleus (1909)

Detector: Fluorescent Screen
Readout Technology: Eyeball

Worked great! But not exactly scalable…







H. SPIELER

Detector: Silicon Strip (1970s)
Readout Technology: Electronics

Major advance in particle tracking. Is it scalable?

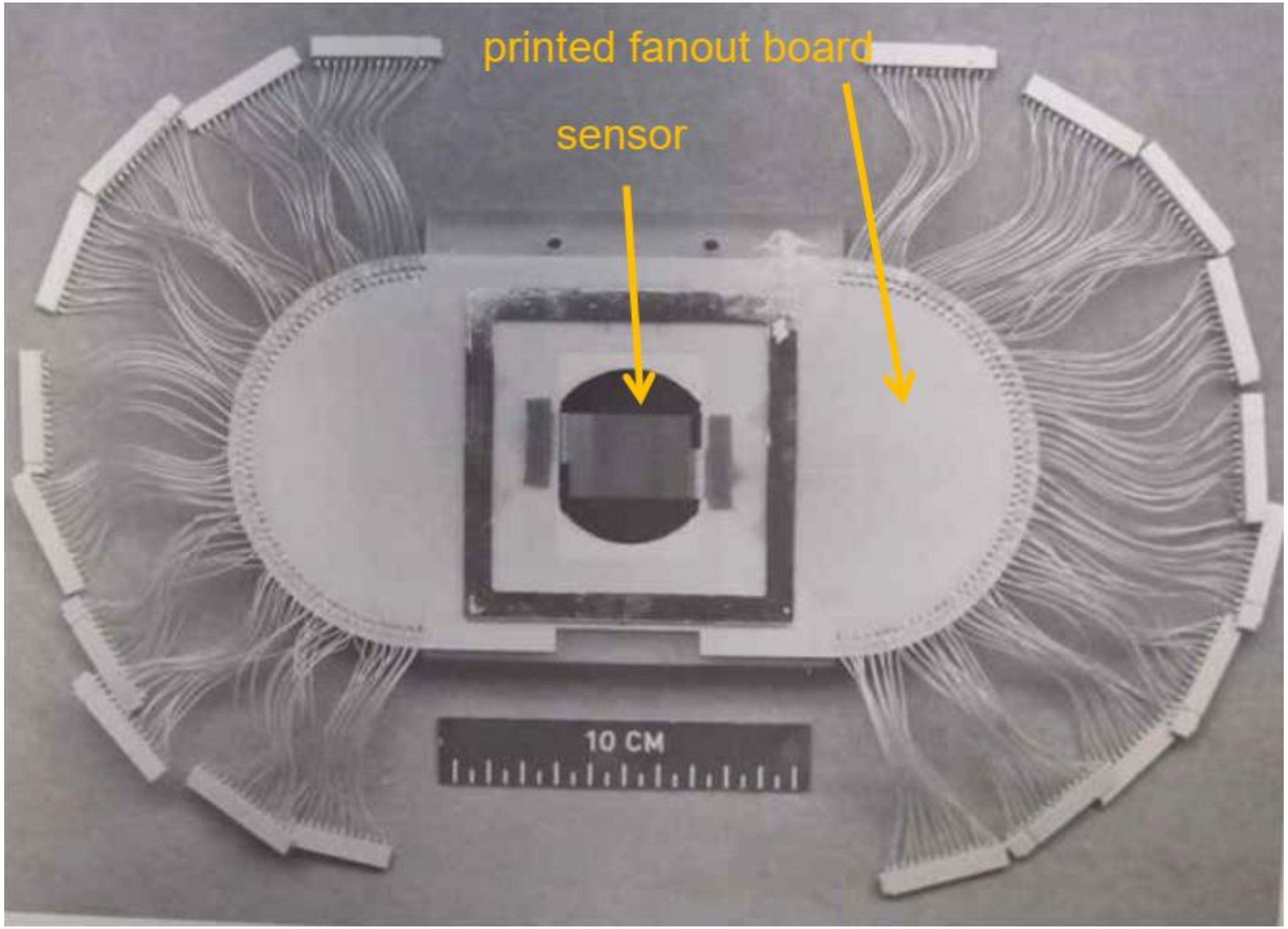
Silicon Strip Readout

State of the art ~ 1980

256 channel strip detector

Readout is implemented using rack of discrete amplifiers and line drivers.

Clearly this is not scalable.



C. HABER

Silicon Strip Readout

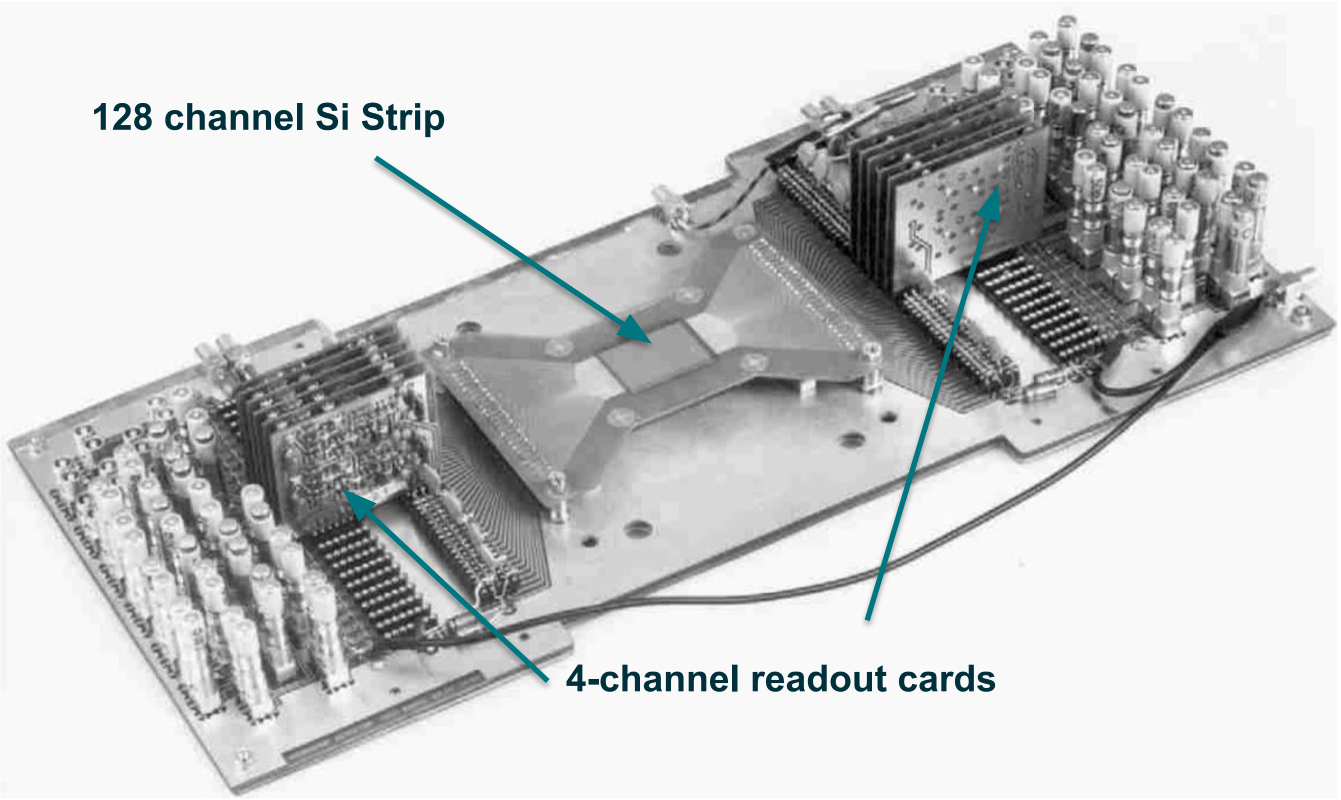
NA11 experiment at CERN (1984) measured charm lifetimes.

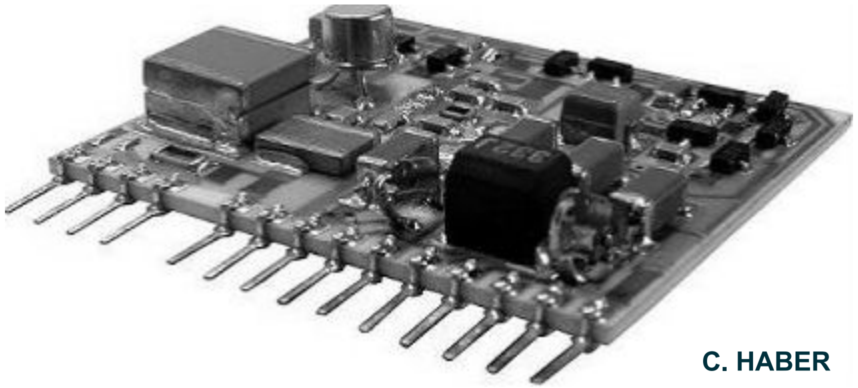
NA11 deployed community's first silicon vertex detector using a 128-channel strip detector module.

Strip detector had 20 μm pitch, but state of the art for discrete readout channels (on PCBs now) was 60 μm.

Strips read out using 32 individual 4-channel boards requiring a LIMO connector per channel.

Better, but this is still not scalable. Great for 1000s of channels. Not so great for millions. End of the road?





Individual readout card
~ 15 mW/channel

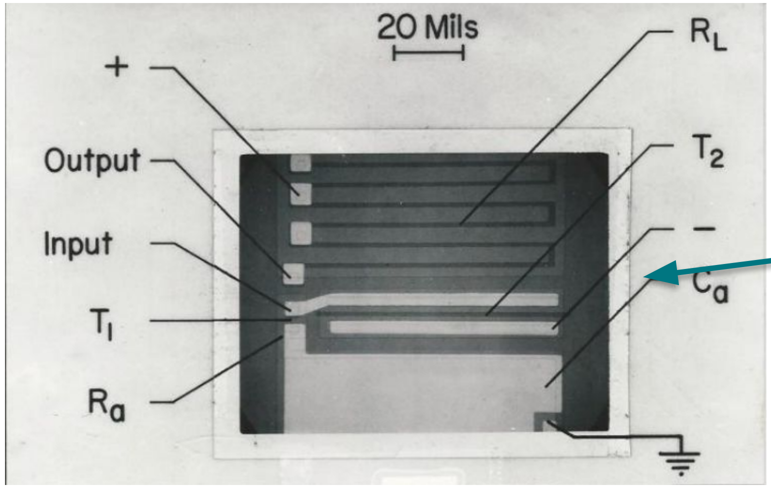
C. HABER

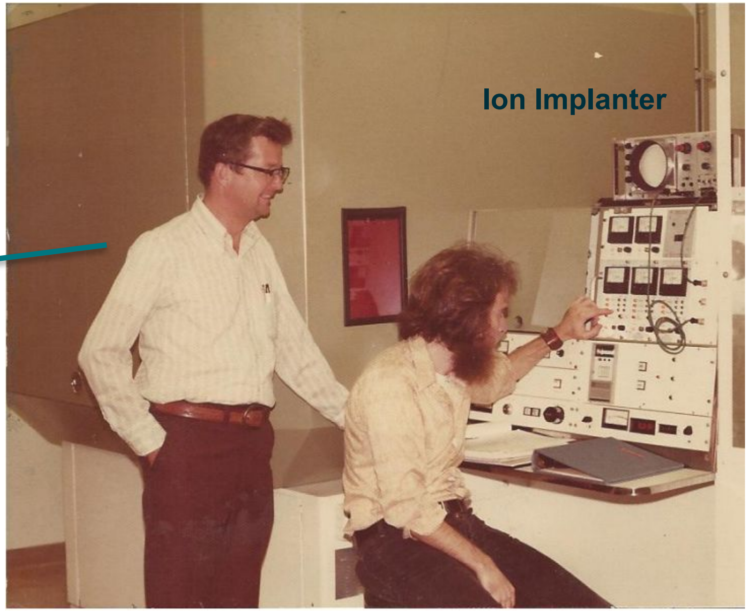
In the dark ages*…

IC Development at UC Berkeley

The Microlab was located on the 4th floor of Cory Hall, facing Hearst Avenue.

Hodges Flip-Flop (1963)



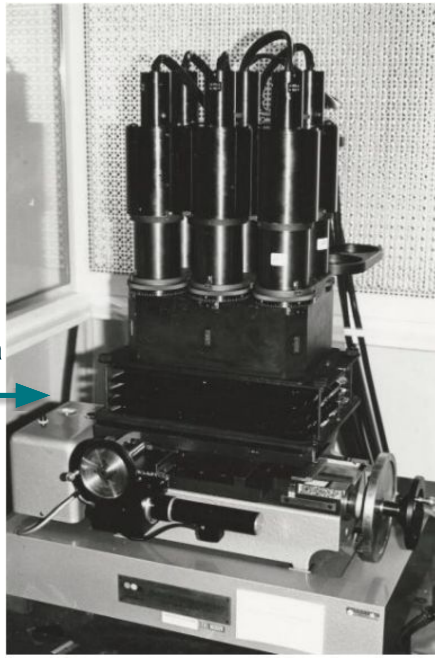


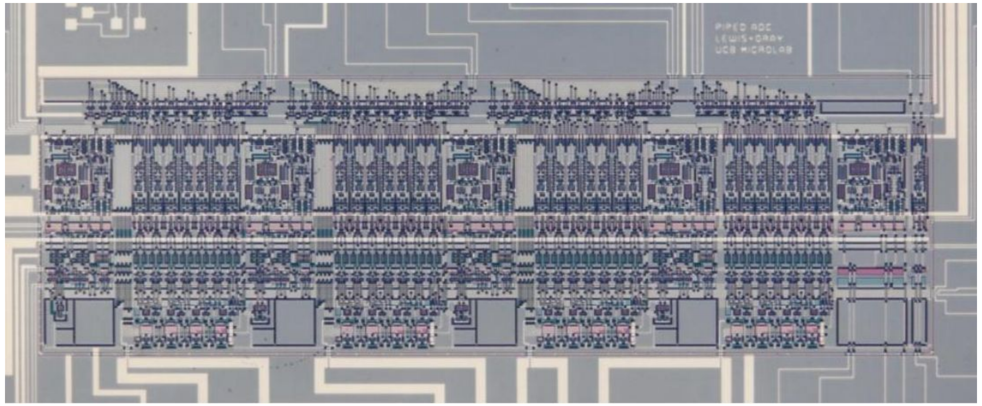
David Hodges William Black

Paul Gray Paul McCreary

First all-MOS ADC (1975)!

Mask Camera





Stephen Lewis – First Pipelined ADC (1986)

*1960s – 1970s

The rise of the Custom ASIC

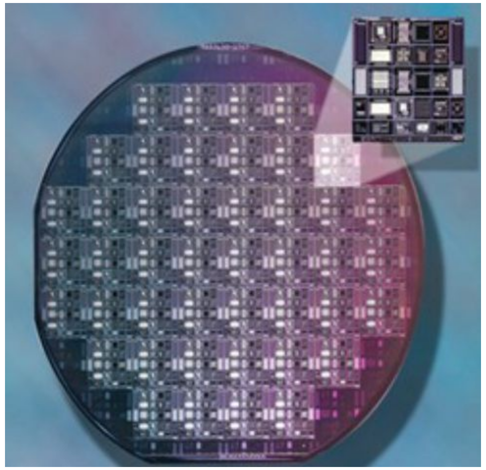
1960s : Only a few Universities made chips

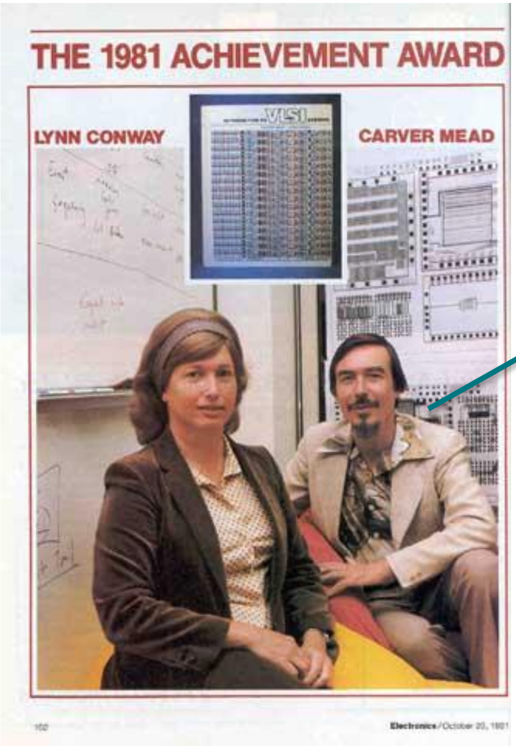
Late 70s : Technology for Multi-Project Wafers (Mead and Conway)

1981 : Founding of MOSIS with DARPA support

1987 : MOSIS commercialized (first large-scale eCommerce application on the Internet)

Also 1987 : TSMC founded (and Fabless Semi industry was born!)



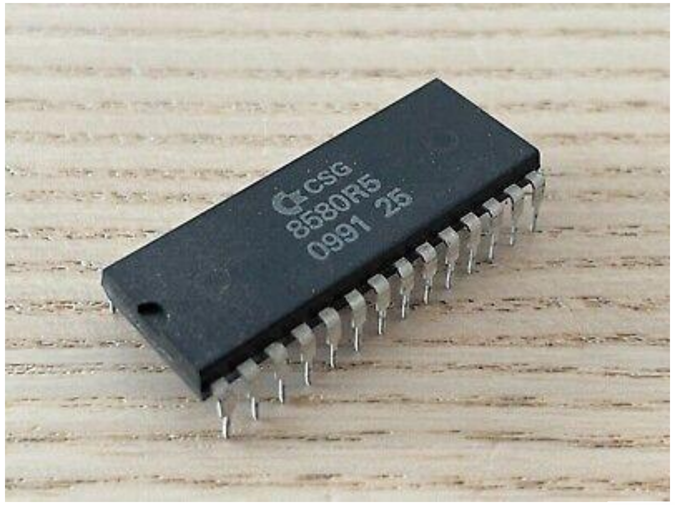


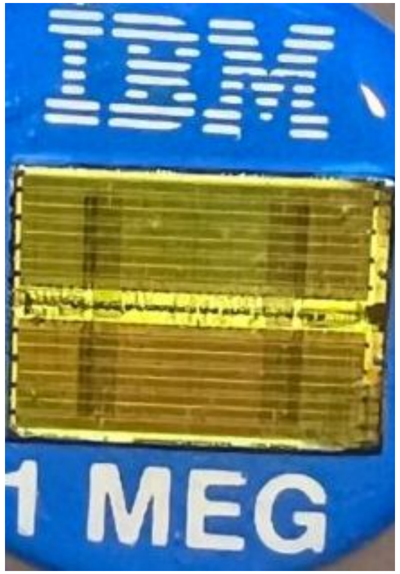
THE MOSIS SERVICE

Trivia alert! The same DARPA program led to the development of the first hardware description language, VHDL.

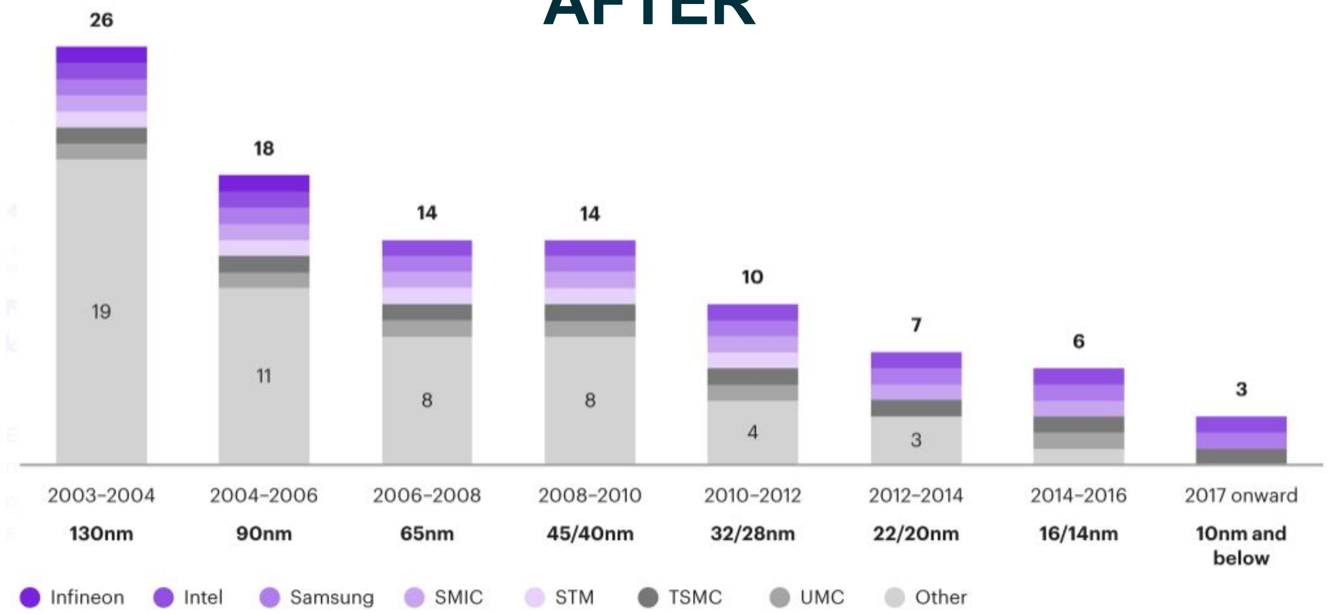
The decline of the “internal fab”

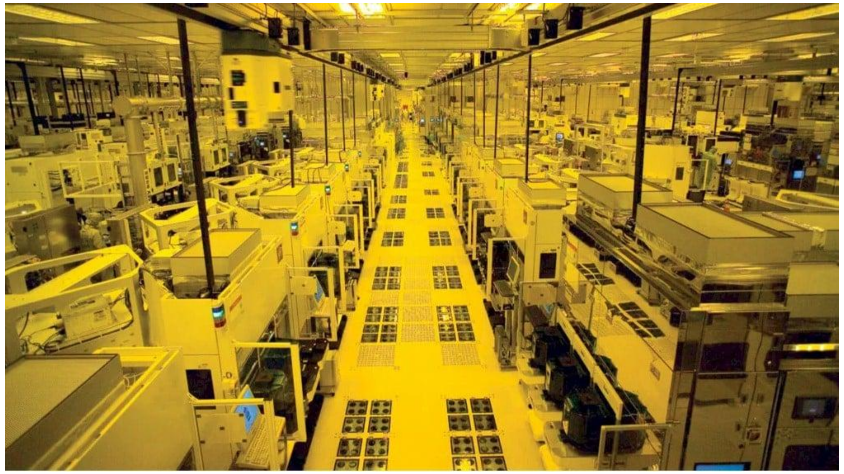
BEFORE





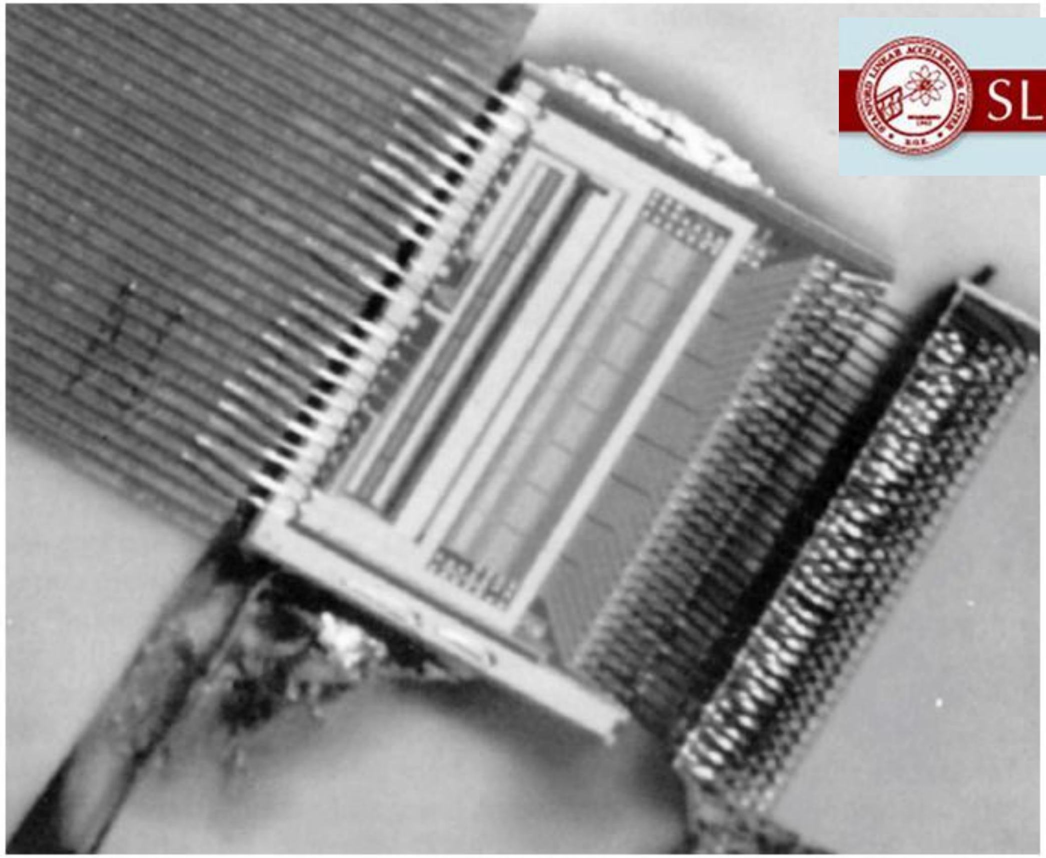
AFTER





First Physics ASICs

Microplex – first custom ASIC for Physics Research

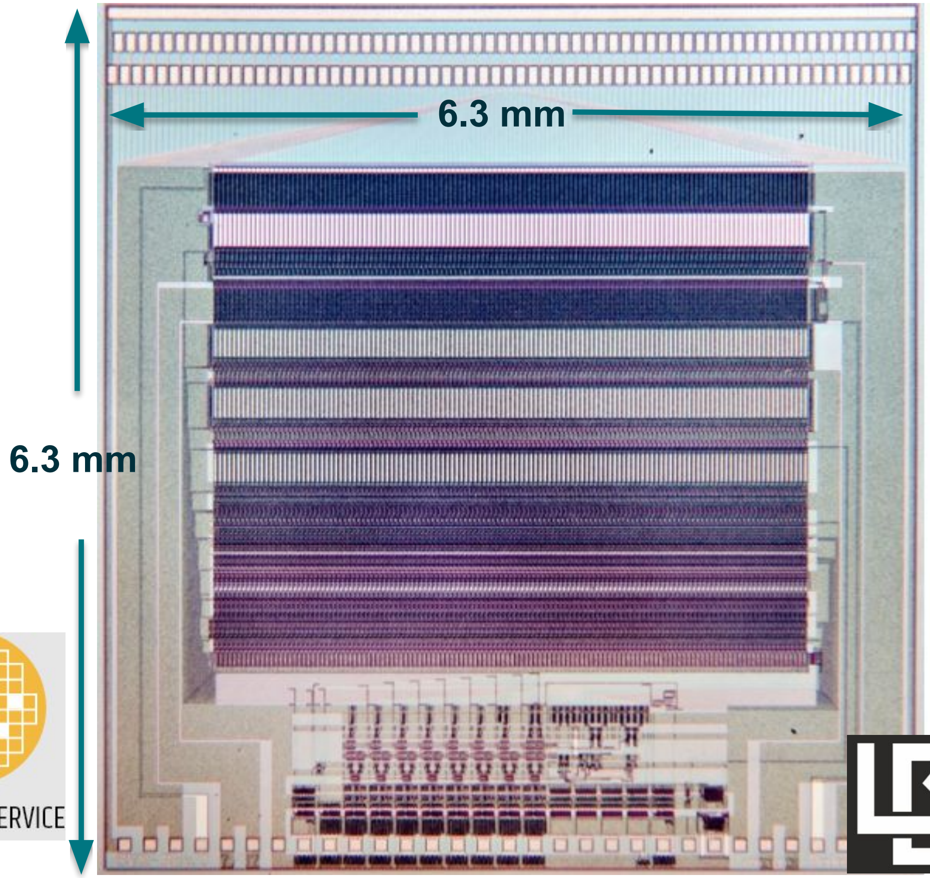


NMOS process (no P-channel devices) - SLAC - 1984

128 channels
3 mW / channel

Walker, Parker, Hyams, Shapiro, "Development of High Density Readout for Silicon Strip Detectors," NIM 226 (1984)

SVX – First CMOS ASIC for Physics Research



11,000 transistors

CDF experiment used 240 SVX chips 30720 channels

Already at discrete limit

CMOS process (with P-channel devices) - LBNL - 1987

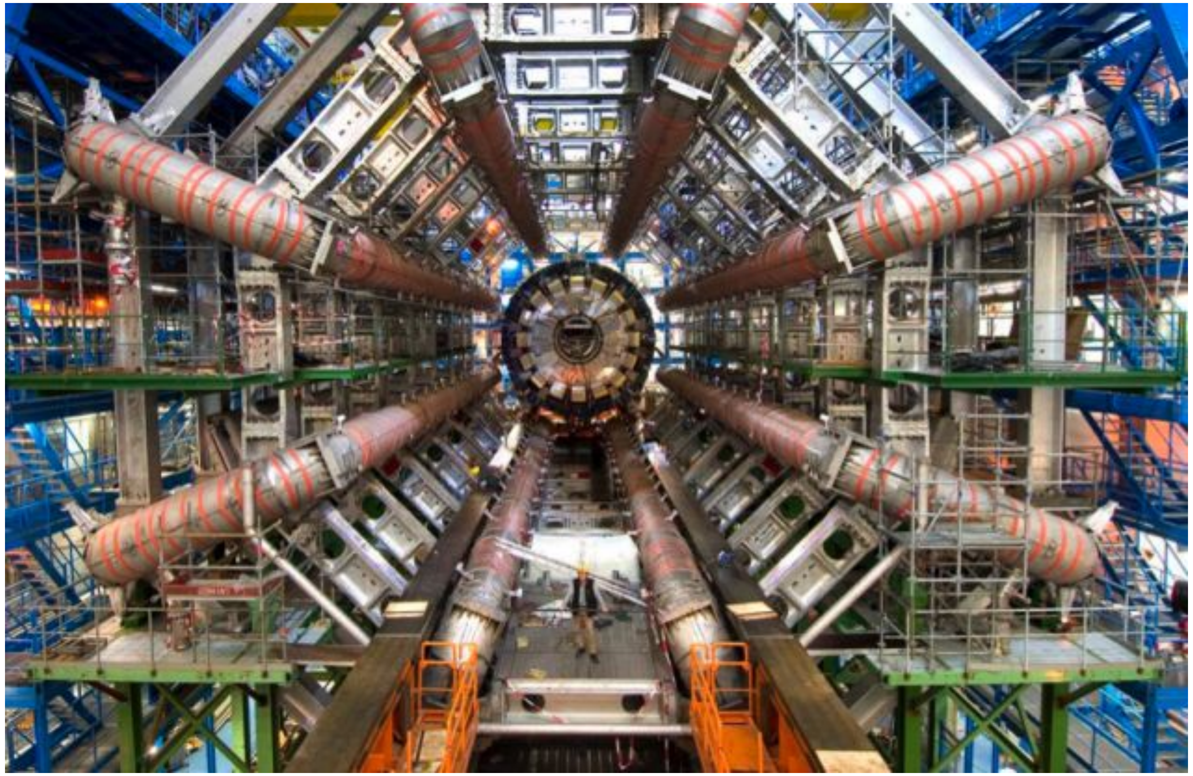
128 channels
1.25 mW / channel

Kleinfelder, et al.; "A Flexible 128-Channel Silicon Strip Detector Instrumentation Integrated Circuit with Sparse Data Readout", TNS 35 (1988)

Challenges for Custom ASICs

Physics experiments often create extreme environments for their readout ASICs

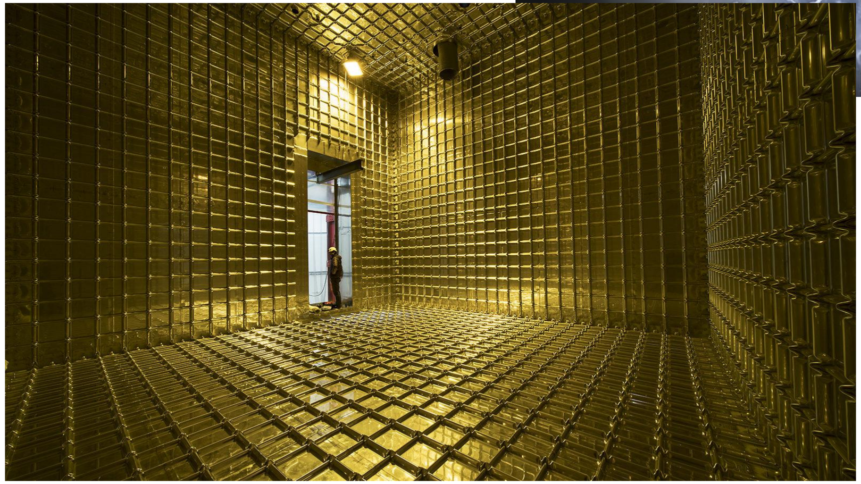
High Radiation



ATLAS Detector

Cold Temperature

Liquid Argon



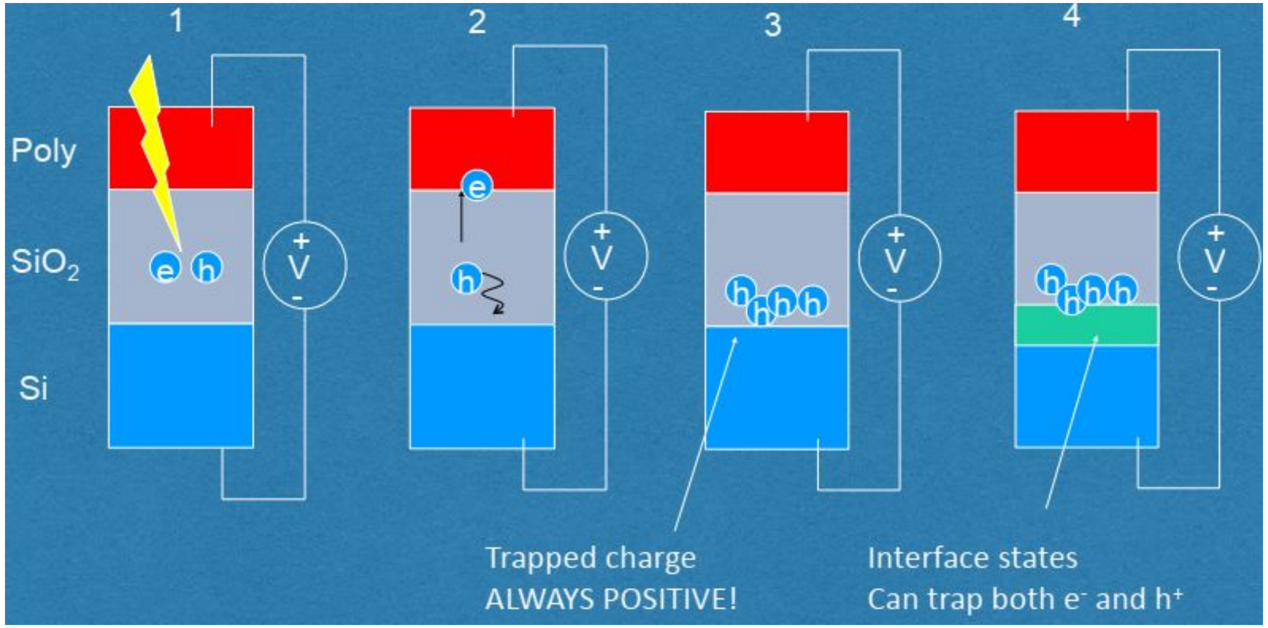
ProtoDUNE LAr TPC

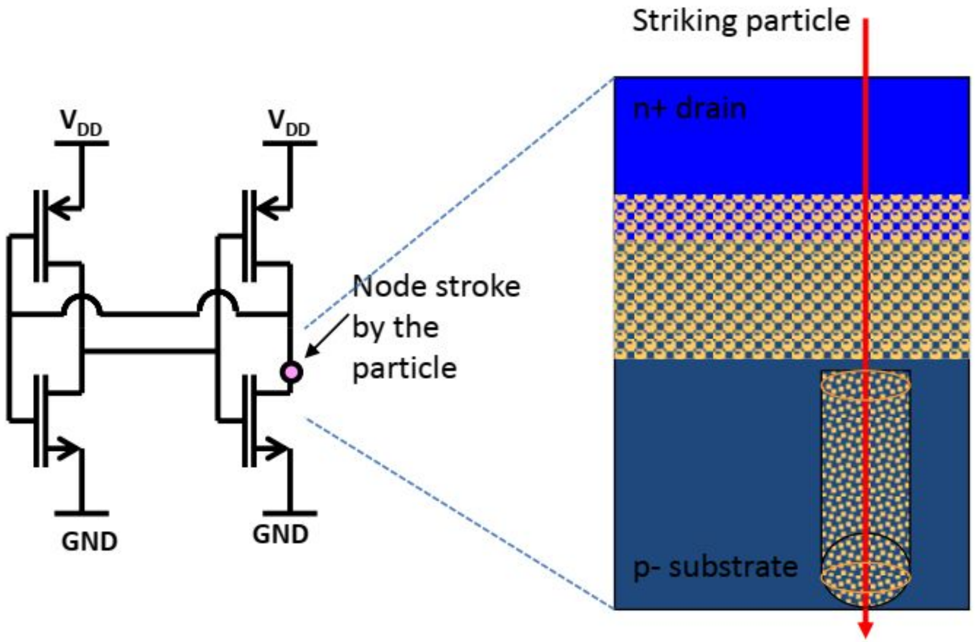
Challenges for Custom ASICs - Radiation

Two main types of radiation damage to integrated circuits that concern us (Single Event Latchup and Single Event Transients of less importance in HEP experiments)

Total Integrated Dose – structural damage to silicon structure that leads to failures

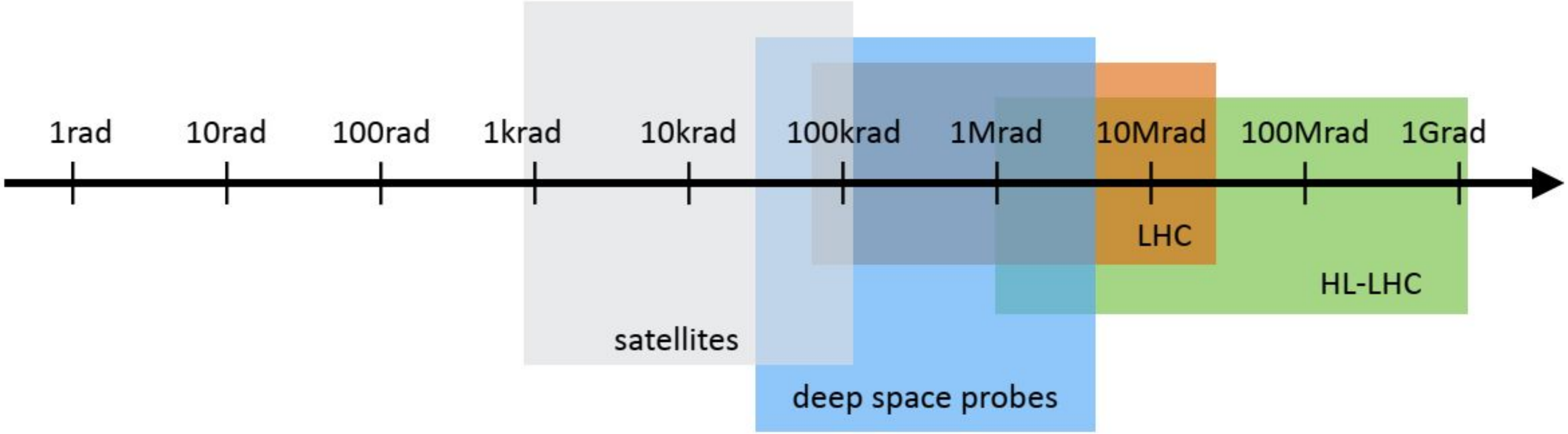
Single Event Upset – transient effects that could modify data or lead to incorrect data

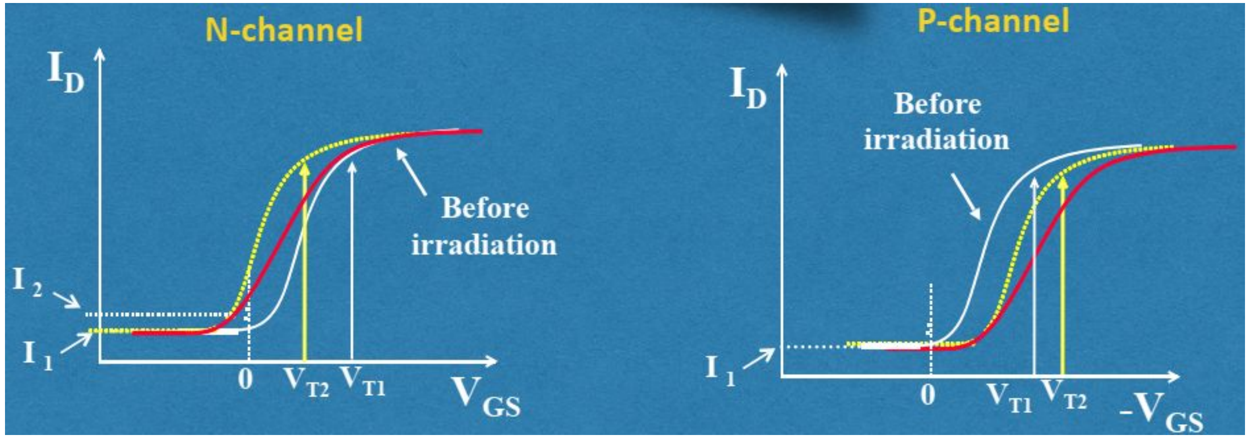




Radiation -- Total Integrated Dose (TID)

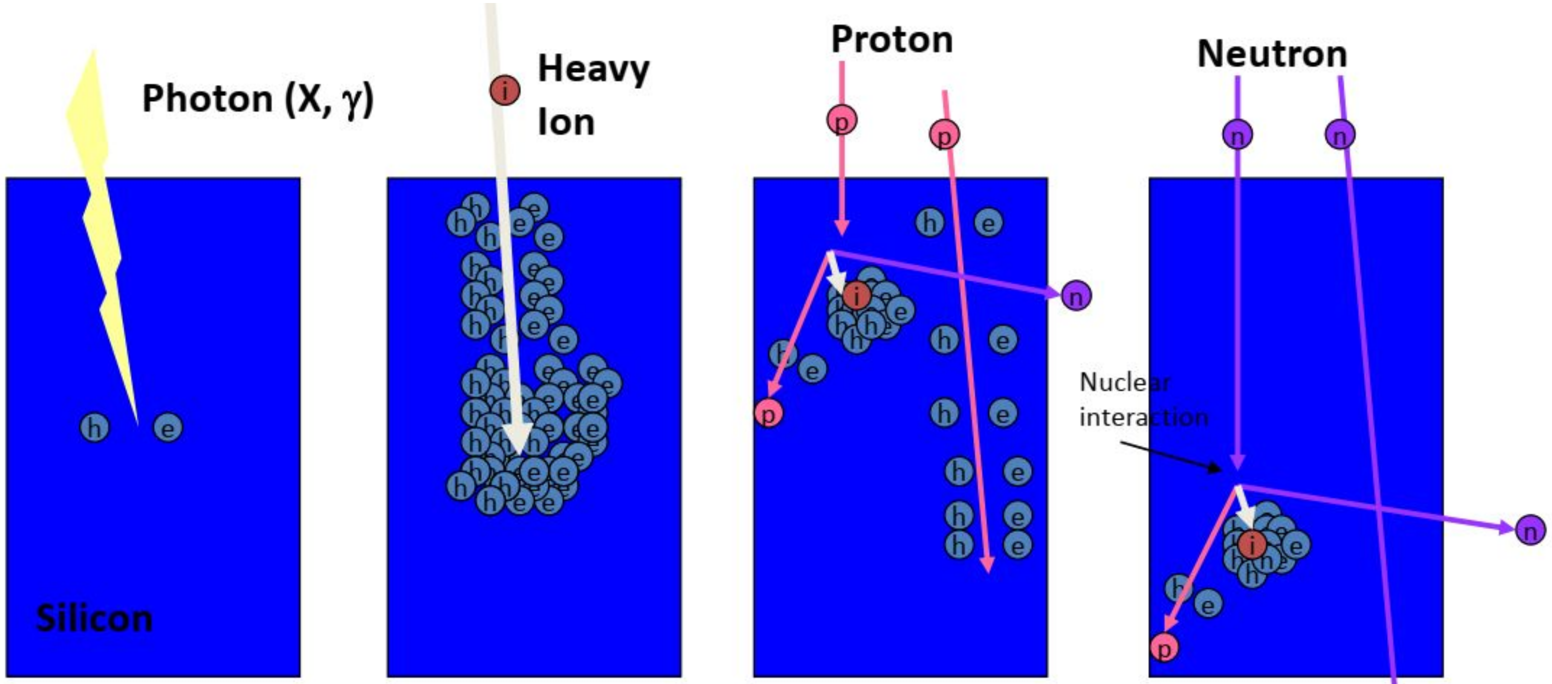
Requirements for TID radiation tolerance for physics far exceed any commercial application





Radiation – Single Event Effects (SEE)

Scaling devices makes ASICs more resilient to TID, but *less* resilient to SEE

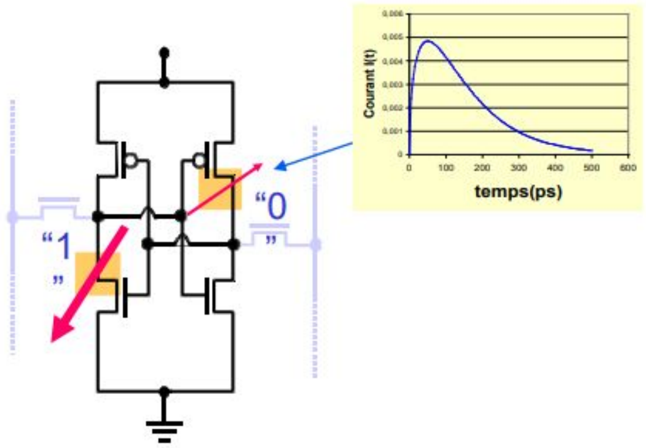


Small density of e-h pairs

Large density of e-h pairs

Small (proton) or no (neutron) density for direct ionization. Possible high density from Heavy Ion produced from nuclear interaction of the particle with Silicon nucleus.

C. Zamantzas



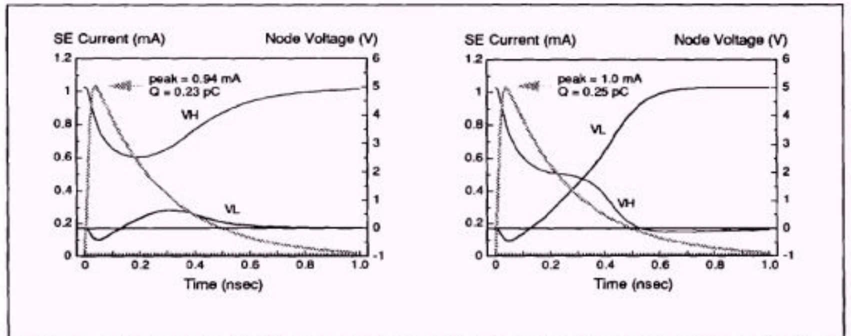
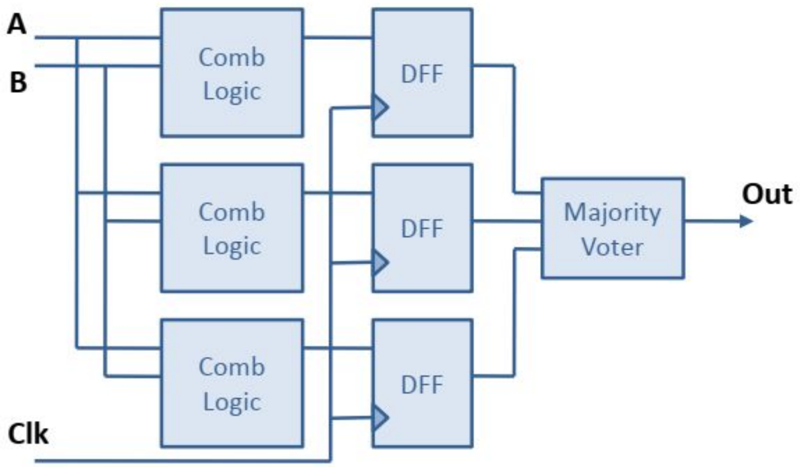


Fig. 4.26 Simulation results showing noupset (left) and upset (right) of the cross-coupled information nodes in a CMOS SRAM cell. In this case, the critical charge is 0.25pC.

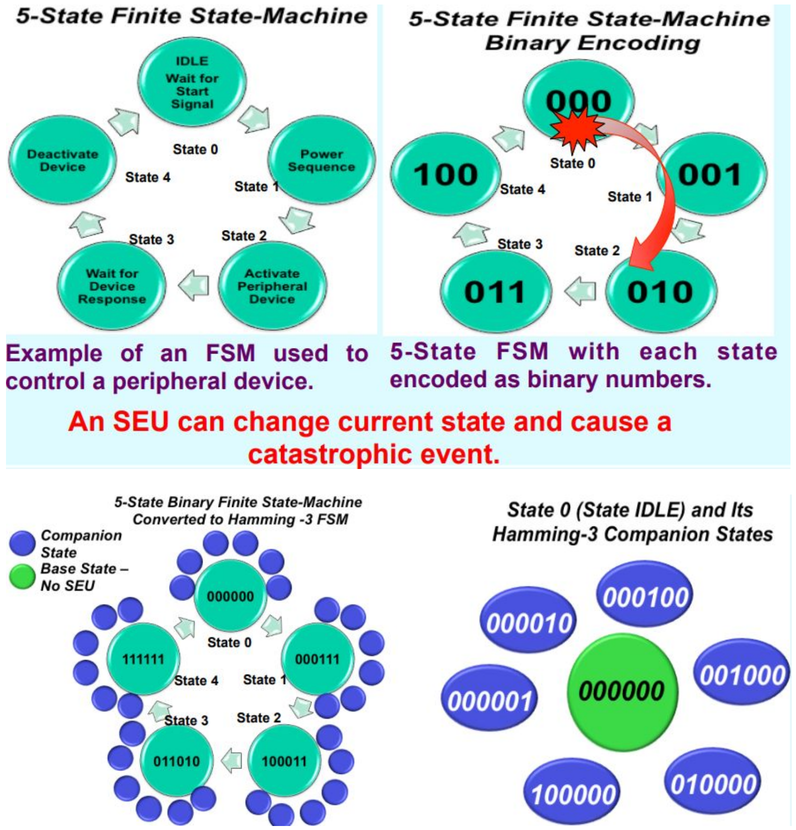
R. Gaillard

Radiation – Single Event Effects (SEE)

Key mitigations: Triple Modular Redundancy (TMR), Hamming encoding, continuous reconfiguration

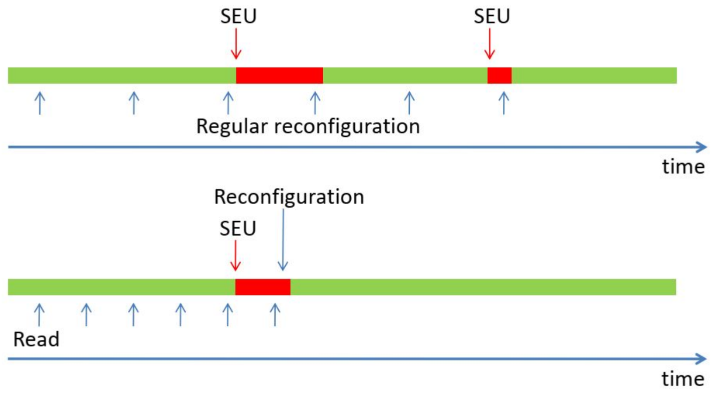


Triple Modular Redundancy (TMR)
- Device level? Circuit? Module?



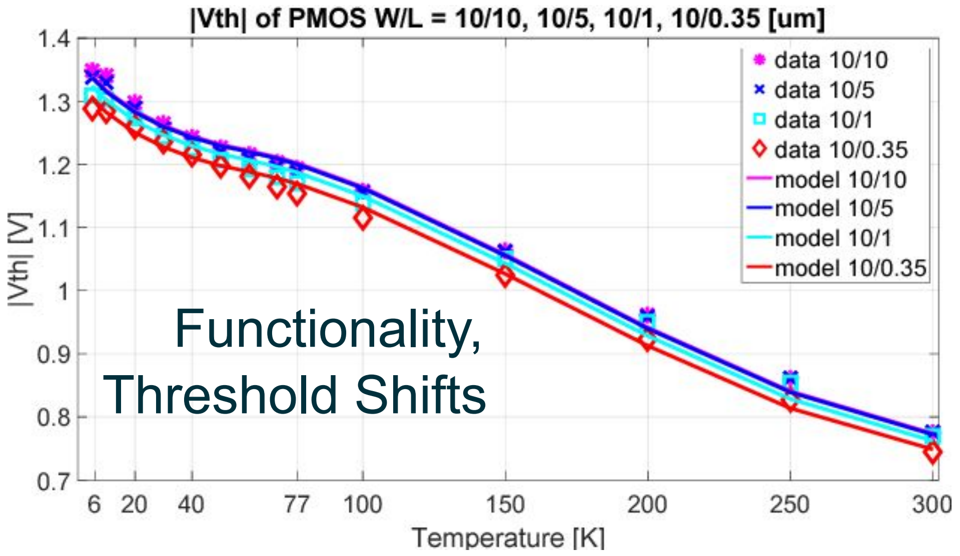
Hamming encoding

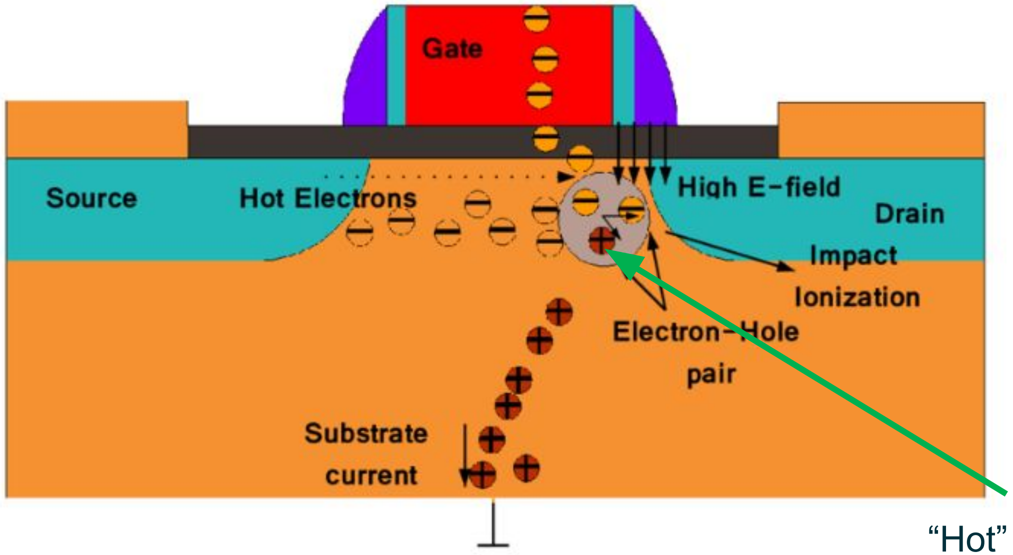
K. Berg



Continuous Reconfiguration

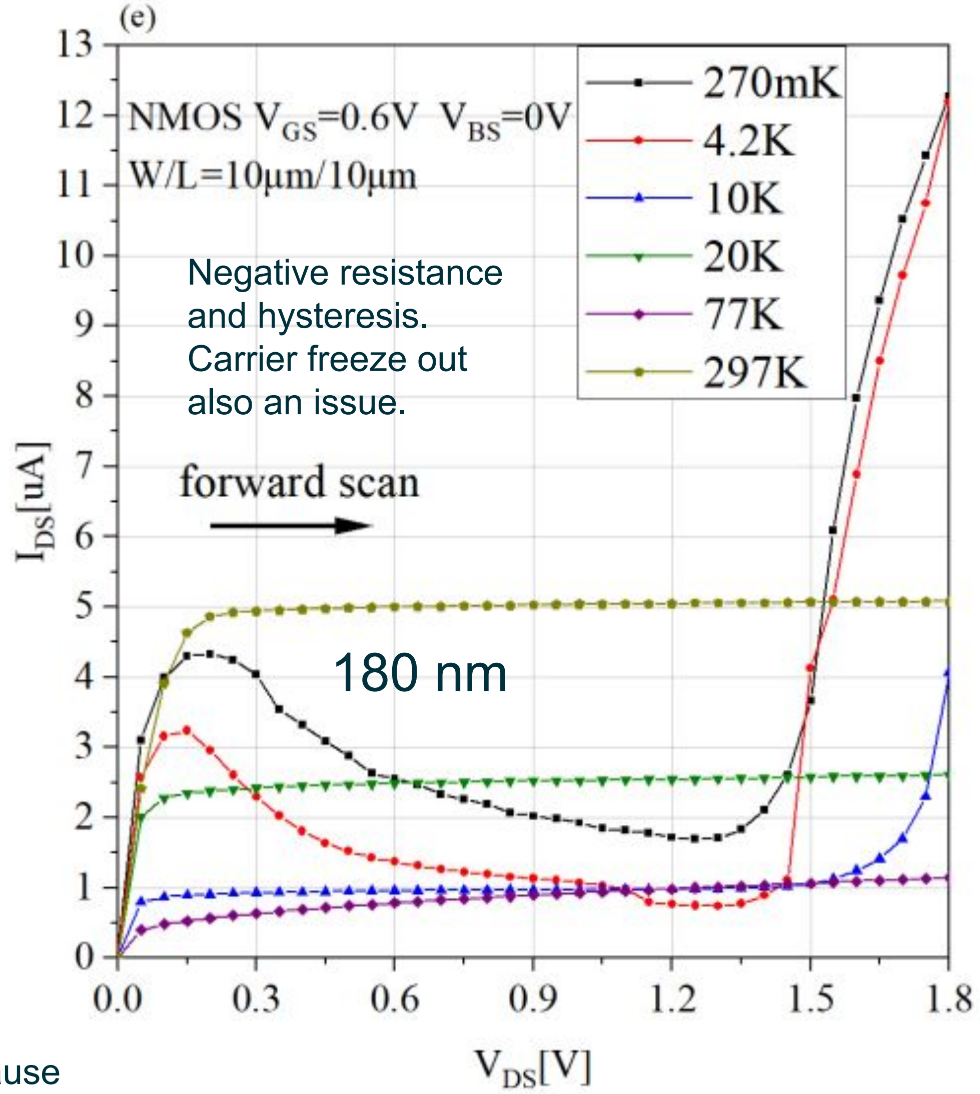
Cryogenic Operation





"Hot" carriers cause early device aging

Reliability and biasing drift



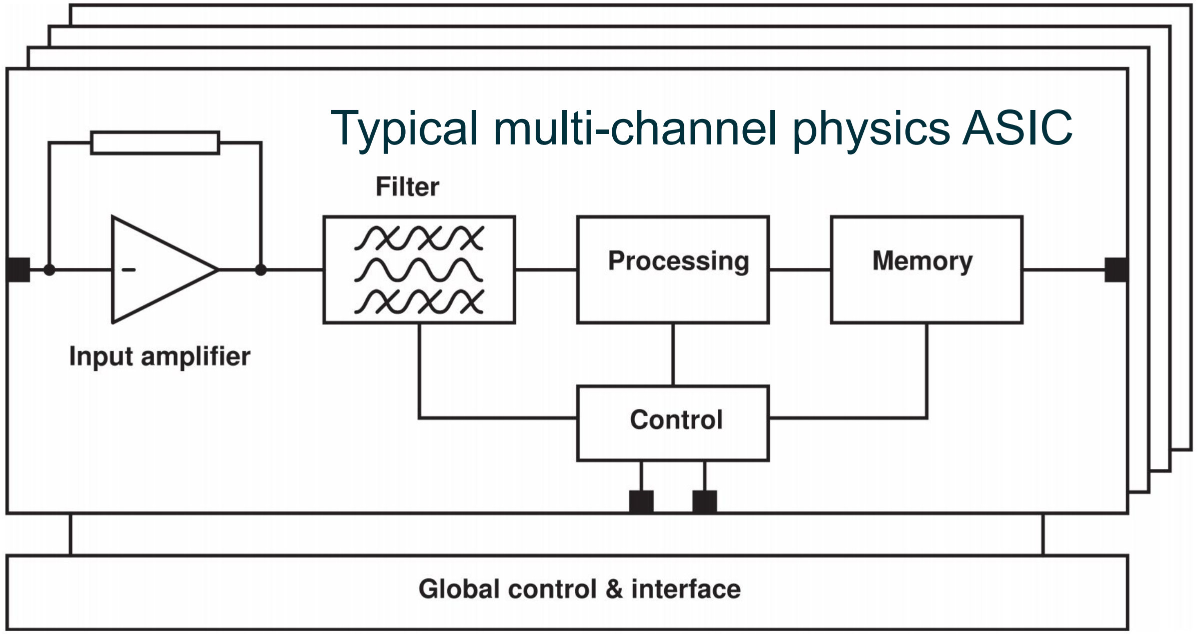
Typical ASICs for HEP

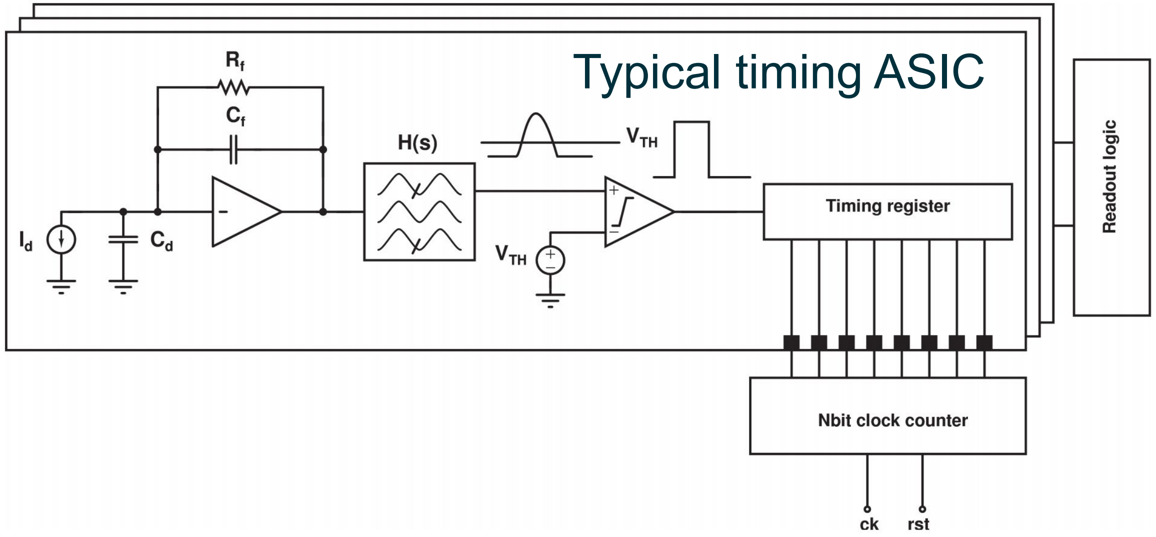
- Typical large physics experiments use capacitive detectors:

  For example, reverse-biased diodes for charged particles, microchannel plates, wires (e.g. in drift chambers), pixels or silicon photomultipliers (SiPMs) for photons (also can be used with scintillators)

- Trend is towards lower noise, improved time and energy resolution, operation in extreme environments, reduced power, and increased number of channels

  Importance of ASICs in physics research is increasing



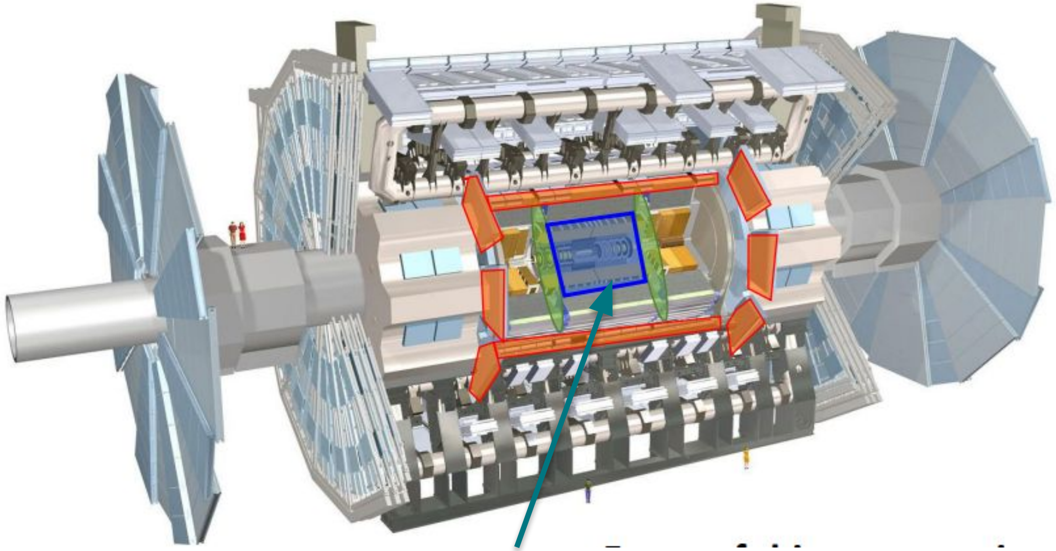


Rivetti "CMOS Front End Electronics for Radiation Detectors"

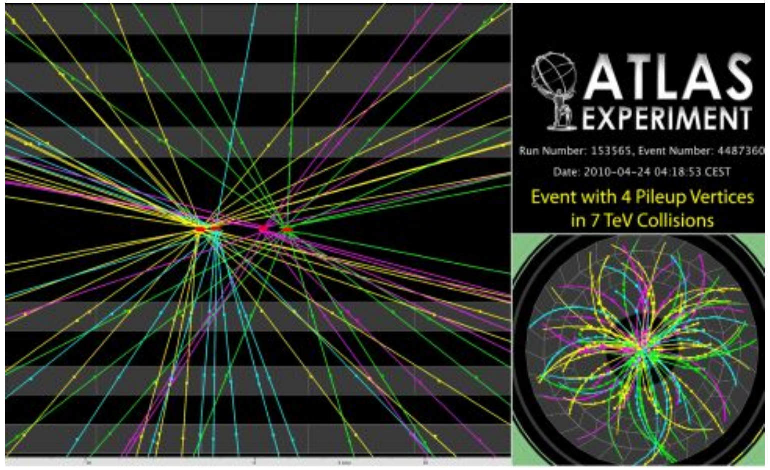
ASIC for Physics Example: ATLAS Inner Tracker (ITk)

Large Hadron Collider – Switzerland and France

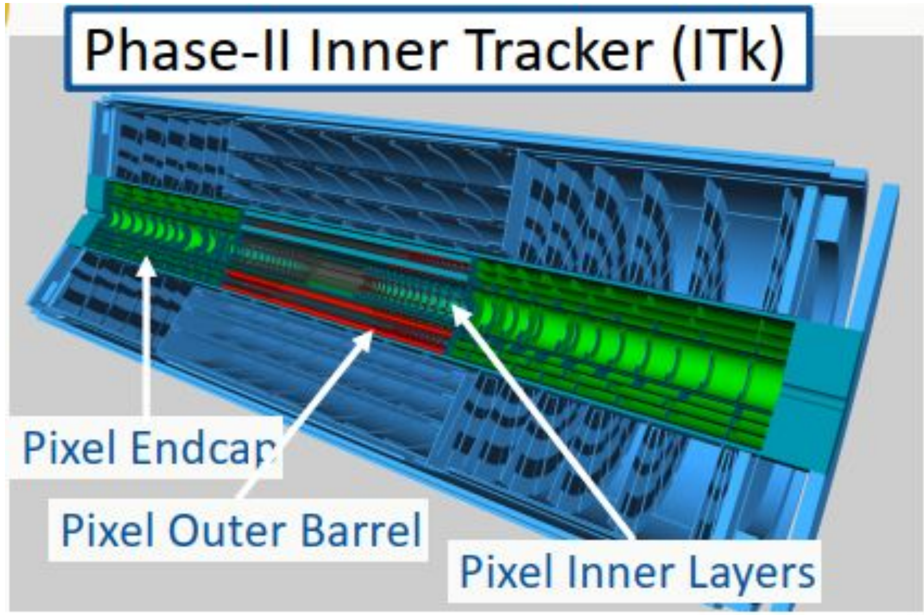
ATLAS Detector



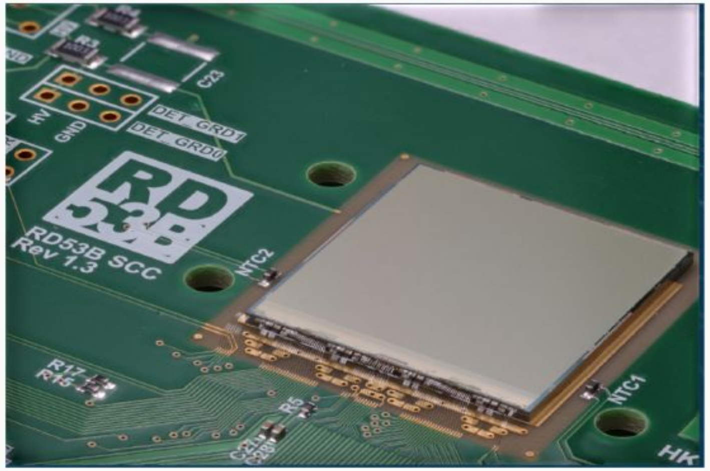
ATLAS Inner Tracking Detector (ITk)

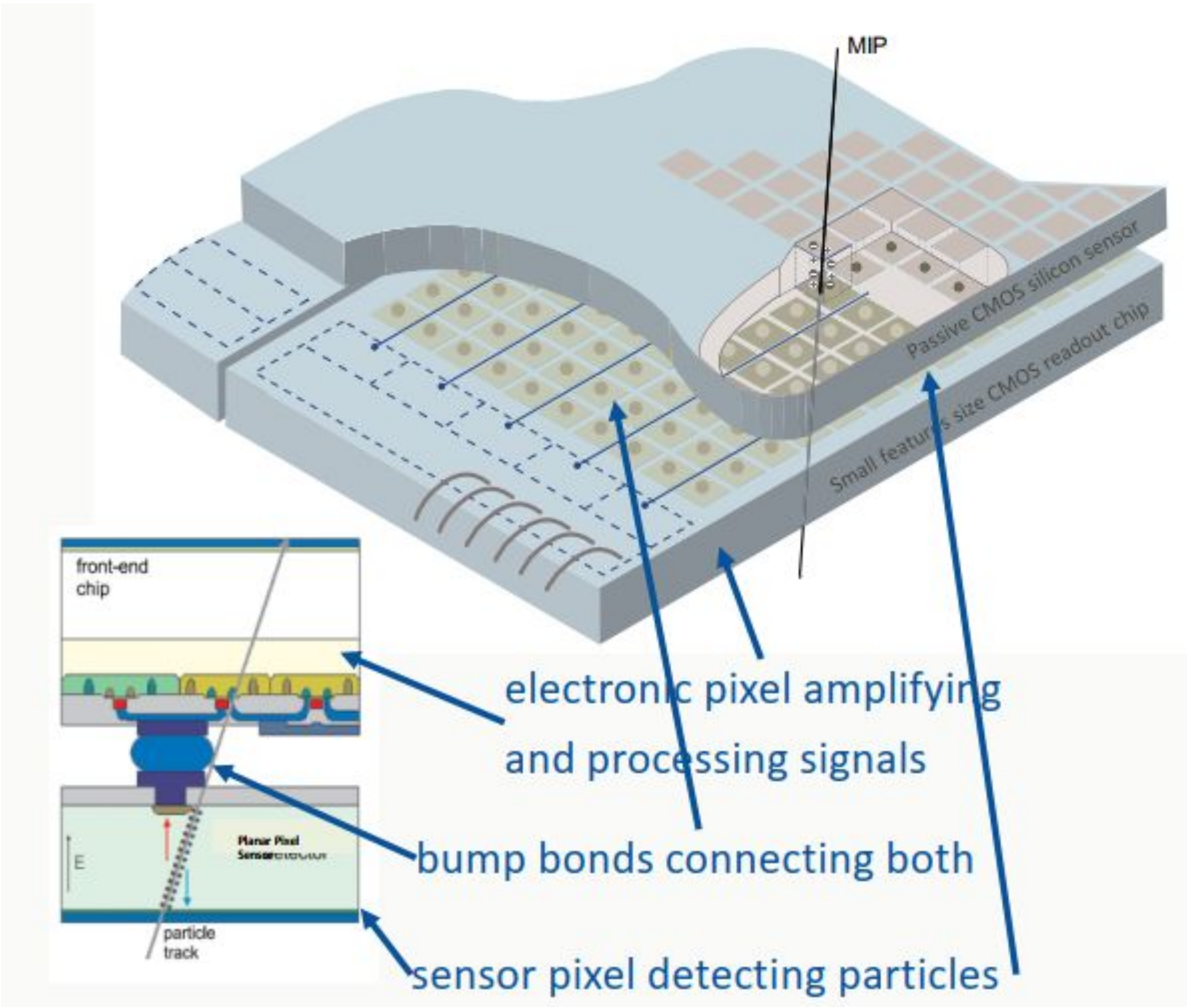


ASIC for Physics Example: ATLAS Inner Tracker (ITk)



RD53B aka ITkPixV1

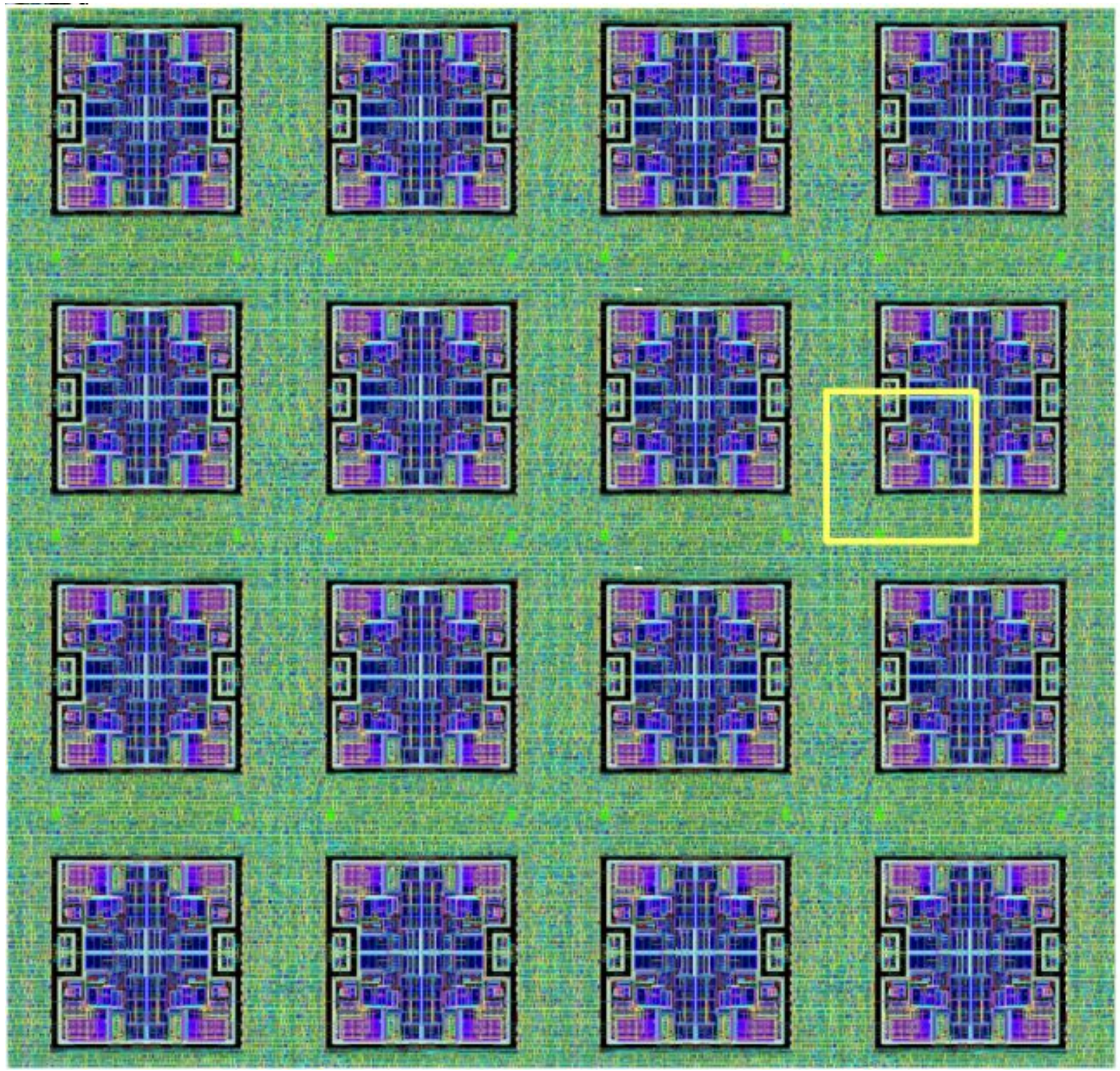




ASIC for Physics Example: ATLAS Inner Tracker (ITk)

RD53A – test chip prior to ITk chip

ITk will have 13 m^2 active area or 1.4 Billion pixels!



Analog island in a sea of synthesized digital logic.

More of a "commercial" design methodology than previous HEP chips.

Silicon Tracker Summary

Name	Microplex	SVX	D-OMEGA	LHC1	FE-I3	FE-14	RD53A	ITkPixv1
Year	1984	1987	1991	1996	2005	2011	2017	2021
Node [µm]	5	3	3	1	0.25	0.13	0.065	0.065
Chip Size [mm]	4.4 x 6.4	6.3x6.3	8.3x6.6	6.6x3.5	10.8x7.6	10.2x19	20x10	20x20
Pixel Size [µm]	47.5 (pitch)	50 (pitch)	70x500	50x500	50x400	50x250	50x50	50x50
Number of Pixels	128 (strips)	128 (strips)	1008	2032	20k	26.9k	79.2k	158.4k
Transistor Count	?	11000	?	800k	3.5M	80M	311M	600M

ASIC for Physics Example: The DUNE Experiment

The Deep Underground Neutrino Experiment (DUNE) is an international science collaboration focused on neutrinos

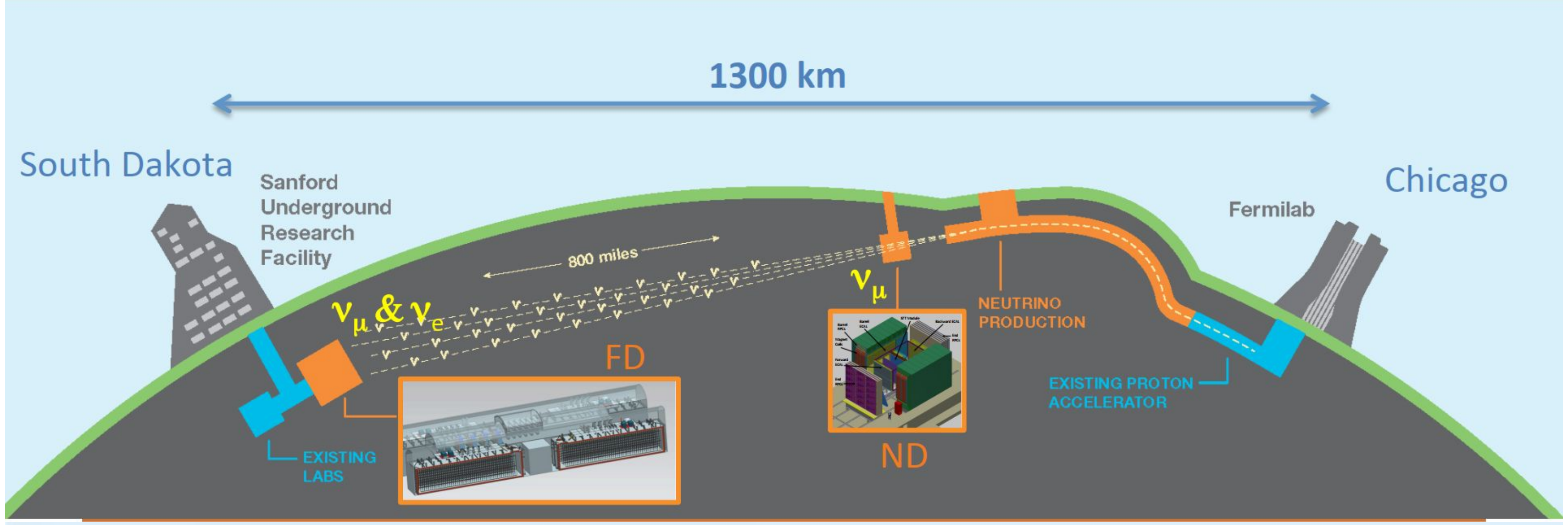
Key Purpose:

Enable the search for CP Violation

Help us understand the matter/antimatter imbalance of the universe.

LBNL is leading the development of the Near Detector (ND) and has an important role in the cold electronics for both the ND and Far Detector (FD).

Neutrinos have a mean-free-path of 60 light years in water so extremely intense beam and dense detector material (Liquid Argon) needed



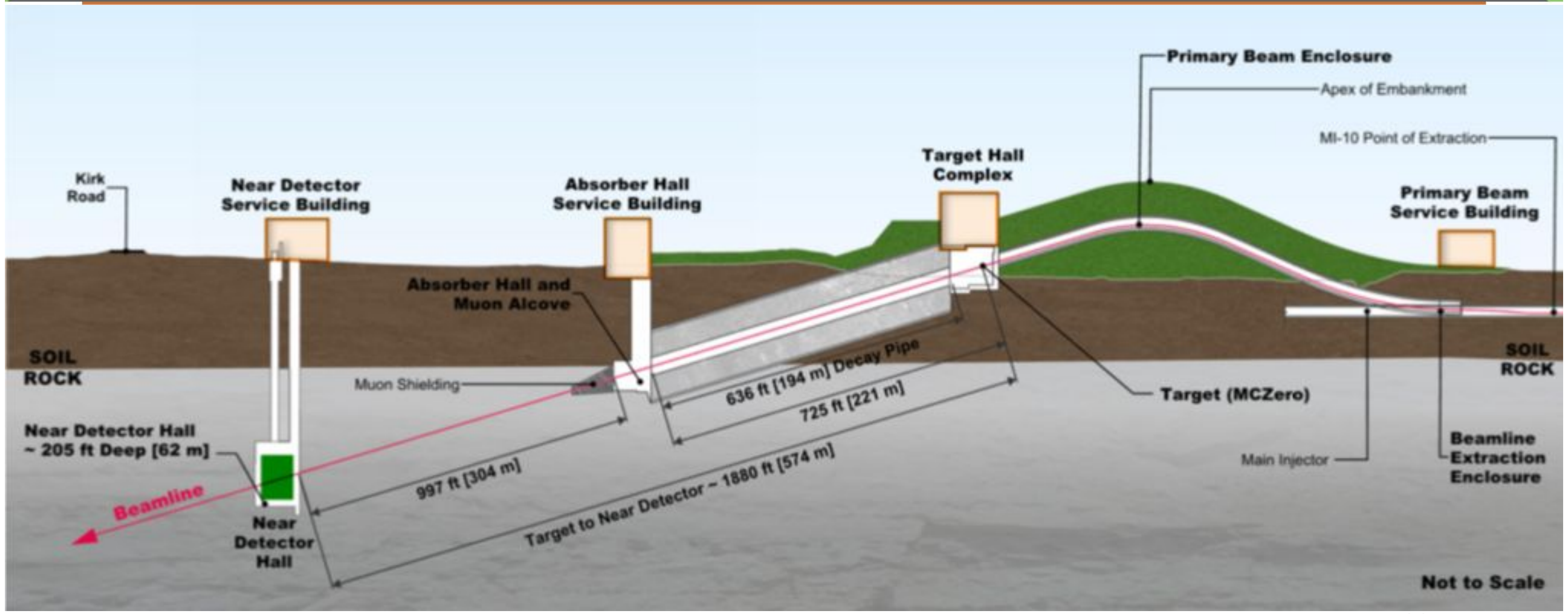
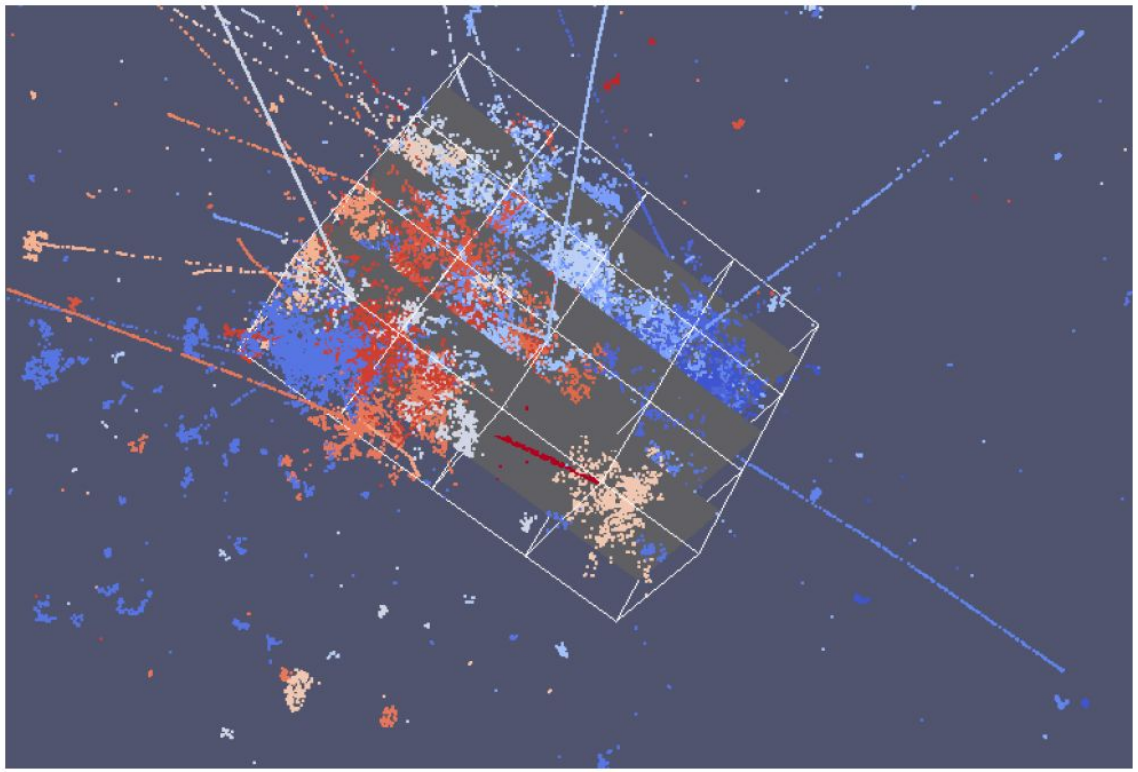
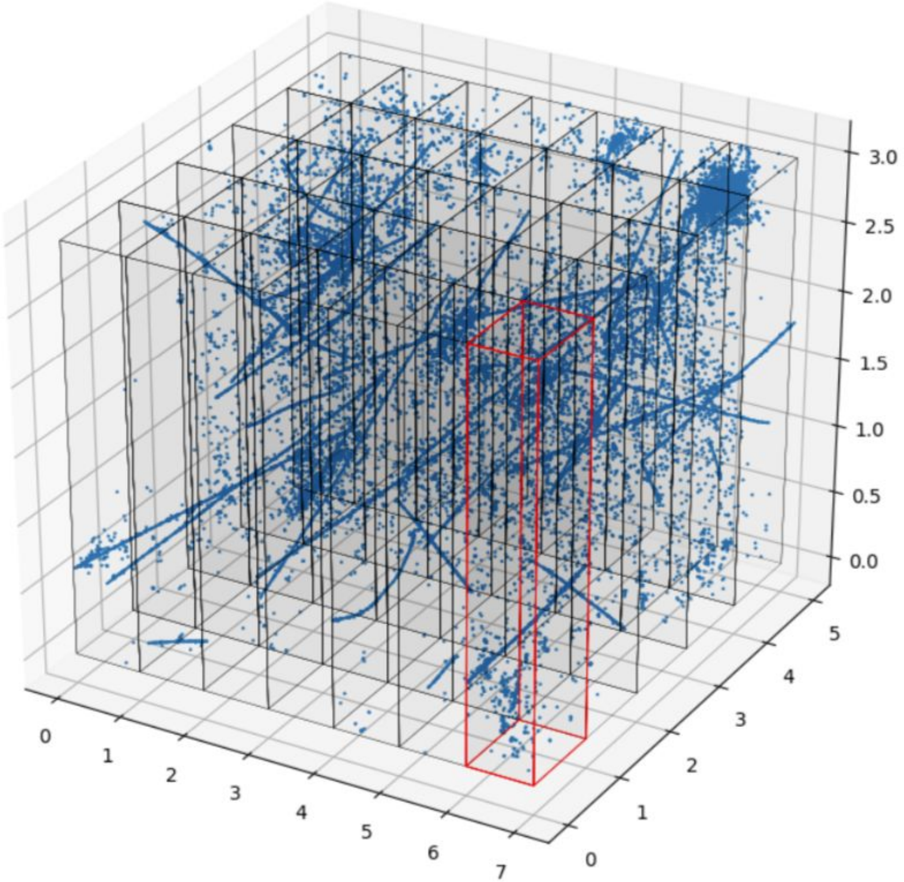


Illustration courtesy LBNF

What is the ND key technical challenge?

The DUNE ND will experience ~10M neutrino events per year. Below is a simulation of neutrino pileup in the ND from a single beam pulse (each color indicates a separate neutrino interaction) not including neutrino background.

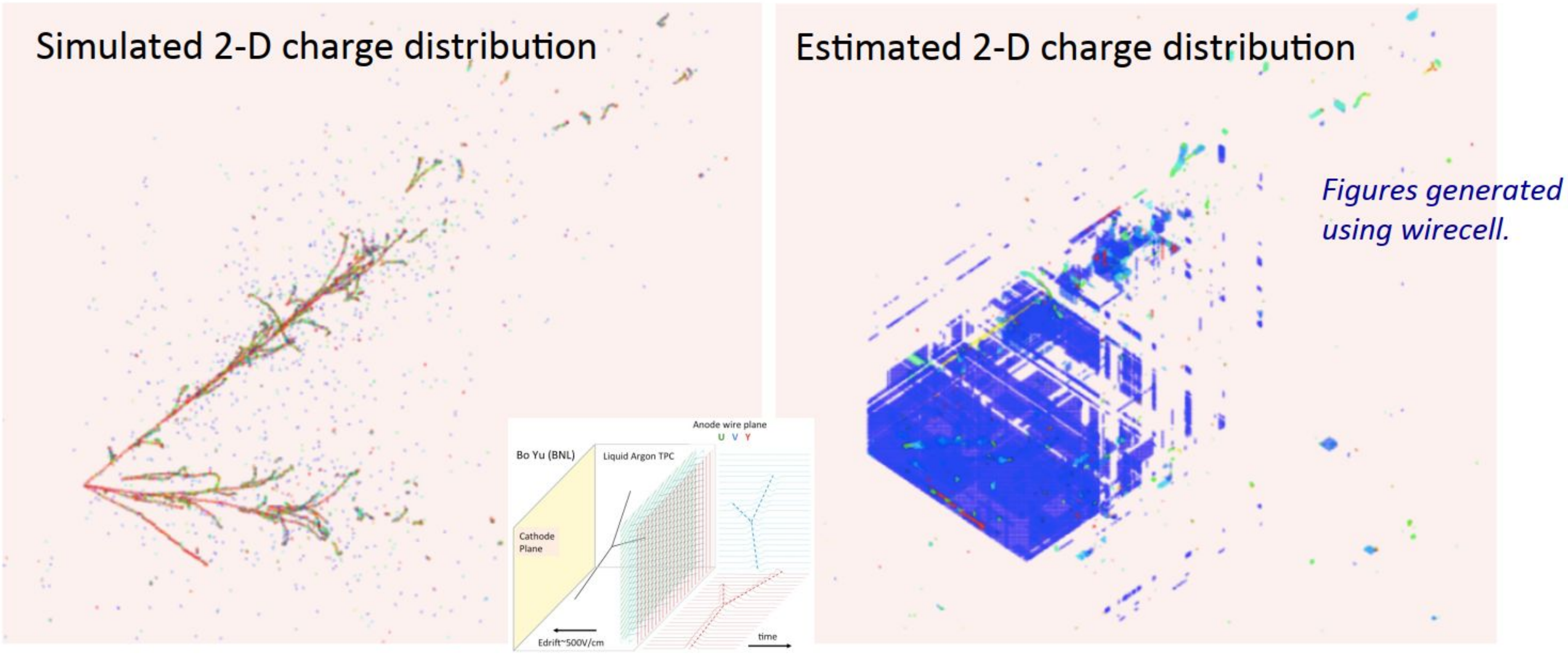




Approximately 50 neutrino interactions per beam spill

What is the ND key technical challenge?

The much larger Far Detector (FD) uses a conventional wire-based liquid Argon (LAr) Time Projection Chamber. Electrons generated by neutrino collisions are drifted in an electric field to wire planes in the cold volume.



3 GeV electron neutrino charge-current interaction in LAr.

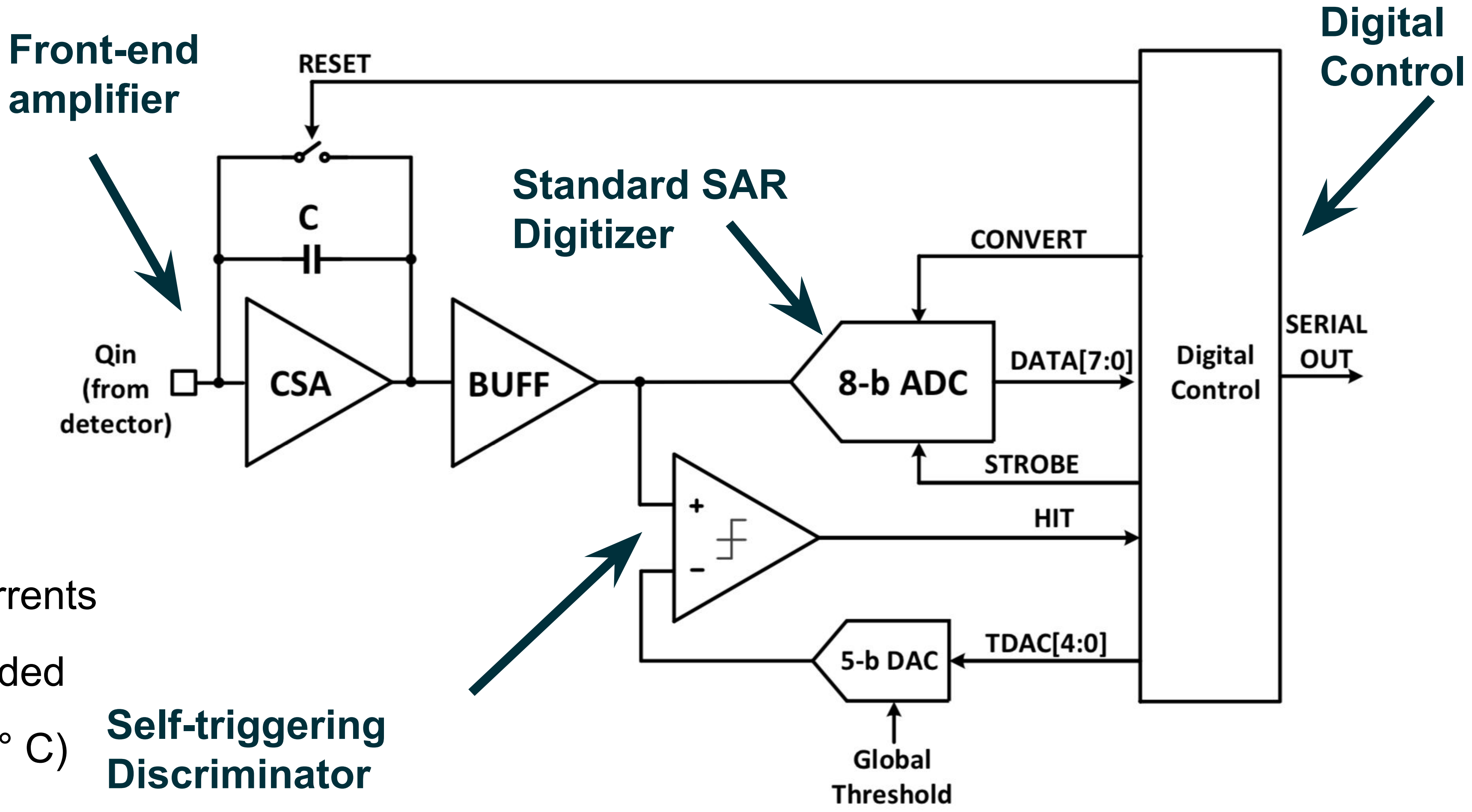
Ambiguity could be a showstopper!

Solution: True 3D readout with a pixelated detector immersed in LAr for the DUNE Near Detector.

LArPix – Liquid Argon Pixel ASIC

Approach: Integrating Amplifier with Self-triggered Digitization and Readout

- 64 channels per ASIC
  - Charge Sensitive Amplifier
  - Discriminator (self trigger)
  - ADC (per channel)
  - Digital Control logic
- Global control logic
- 2k FIFO
- On chip references and bias currents
- Only decoupling capacitors needed
- Immersed in Liquid Argon (-184° C)



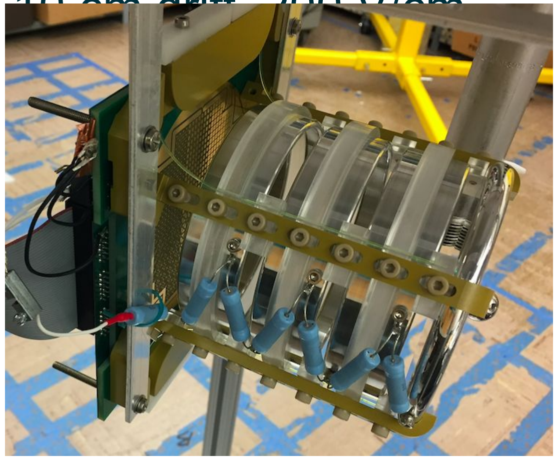
Achieve low power: avoid digitization and readout of mostly quiescent data.

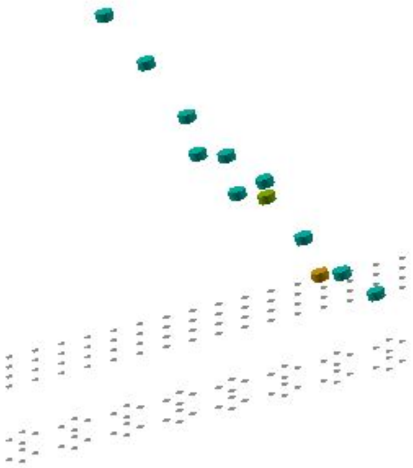
Demonstration of cosmic ray detection at increasing scales

Feb 2018:

128-pixel system @ LBNL

10 cm drift, 200 V/cm

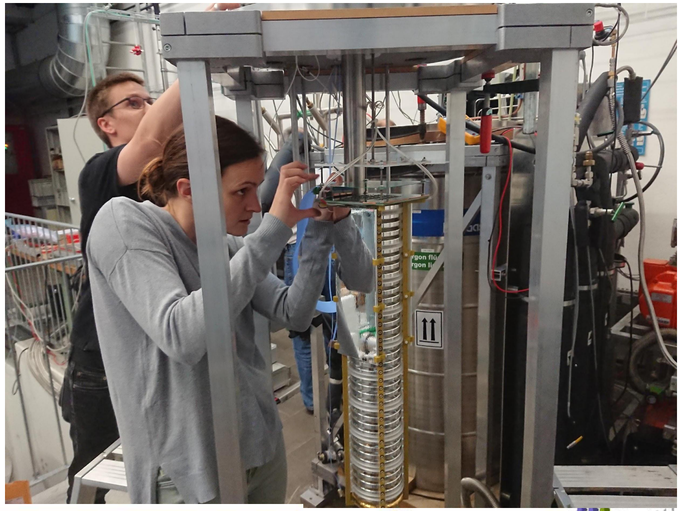


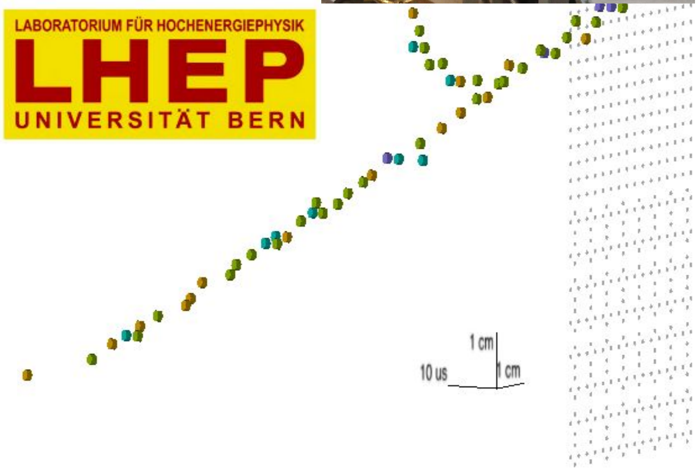


Apr 2018:

512-pixel system @ Bern

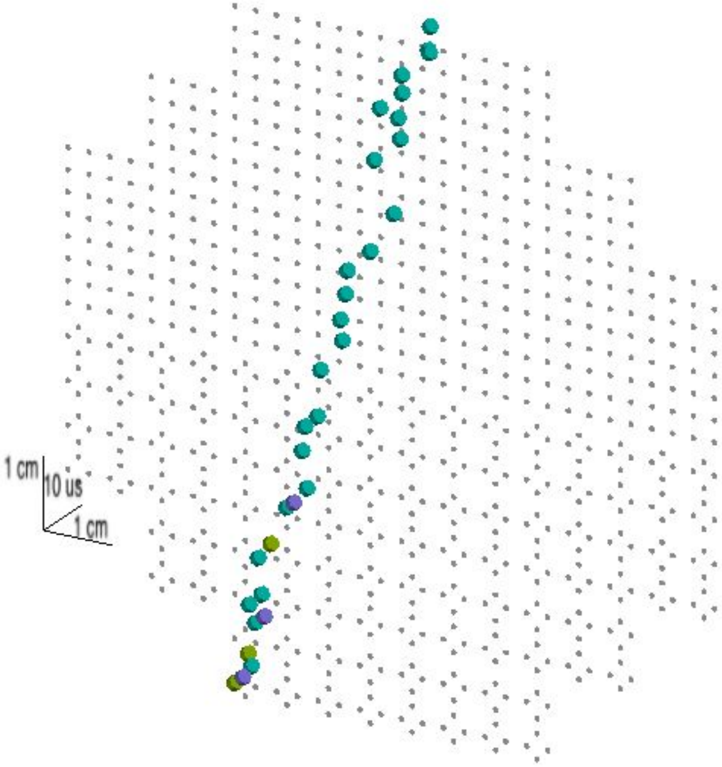
60 cm drift, 1 kV/cm





May 2018:

832-pixel system @ LBNL



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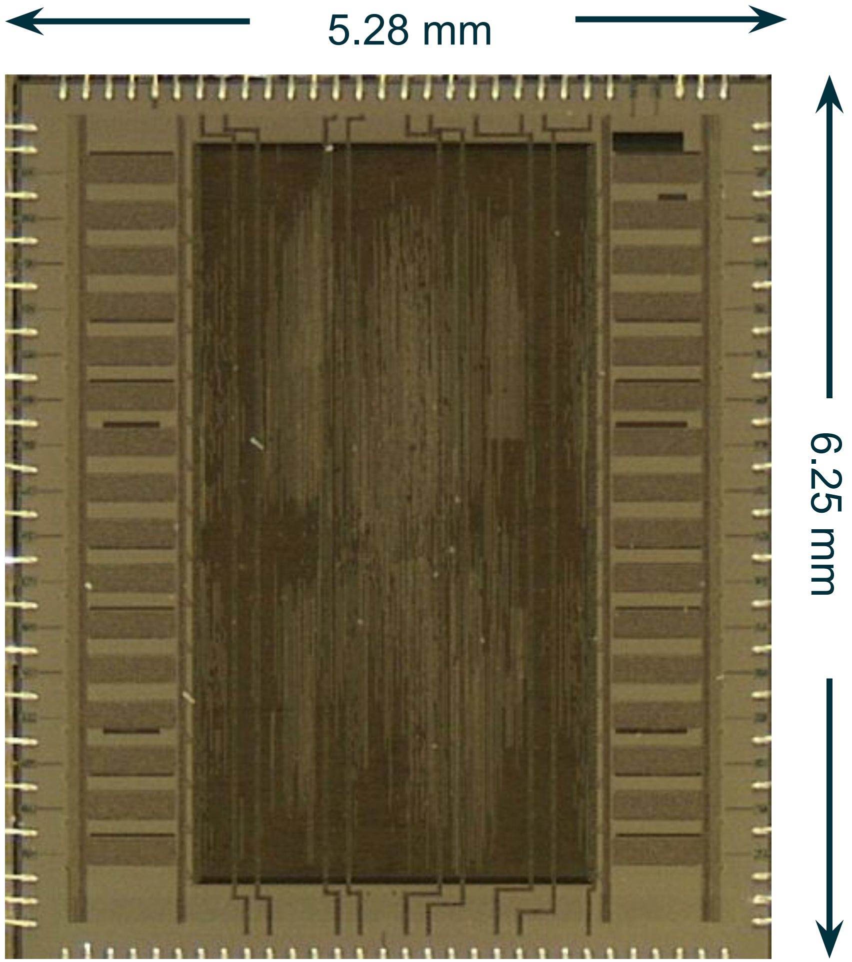
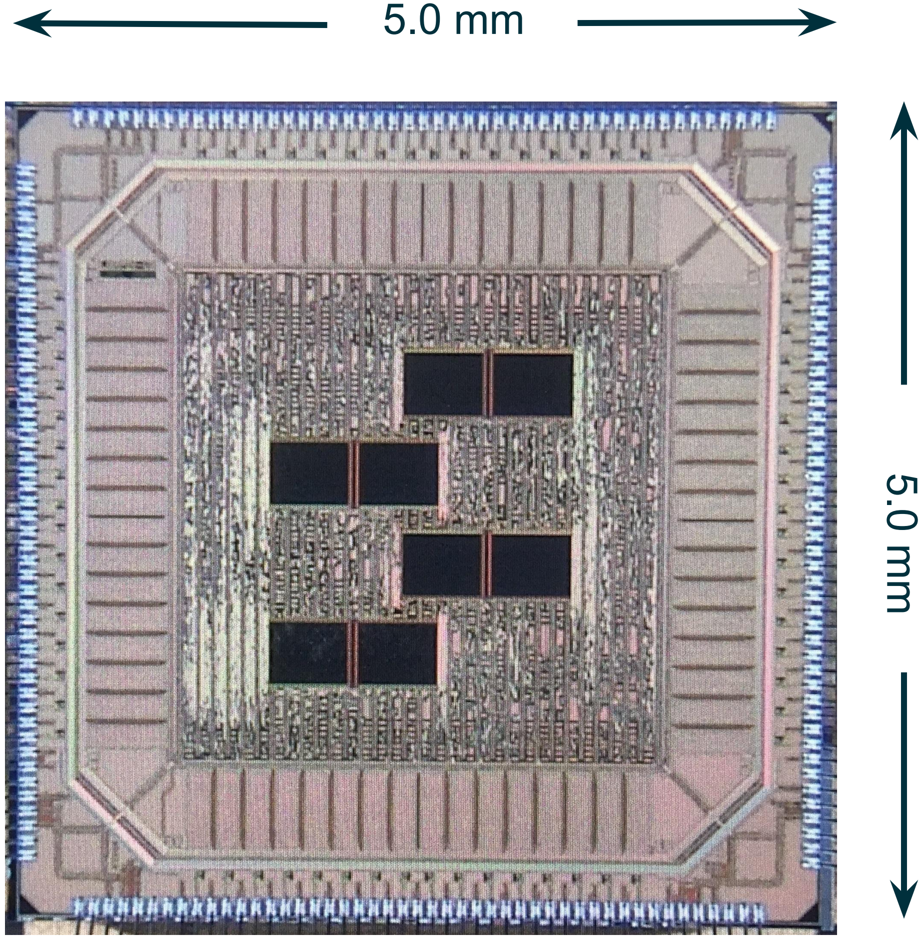
Quick Design Iteration Continuous Improvement



LArPix-v1

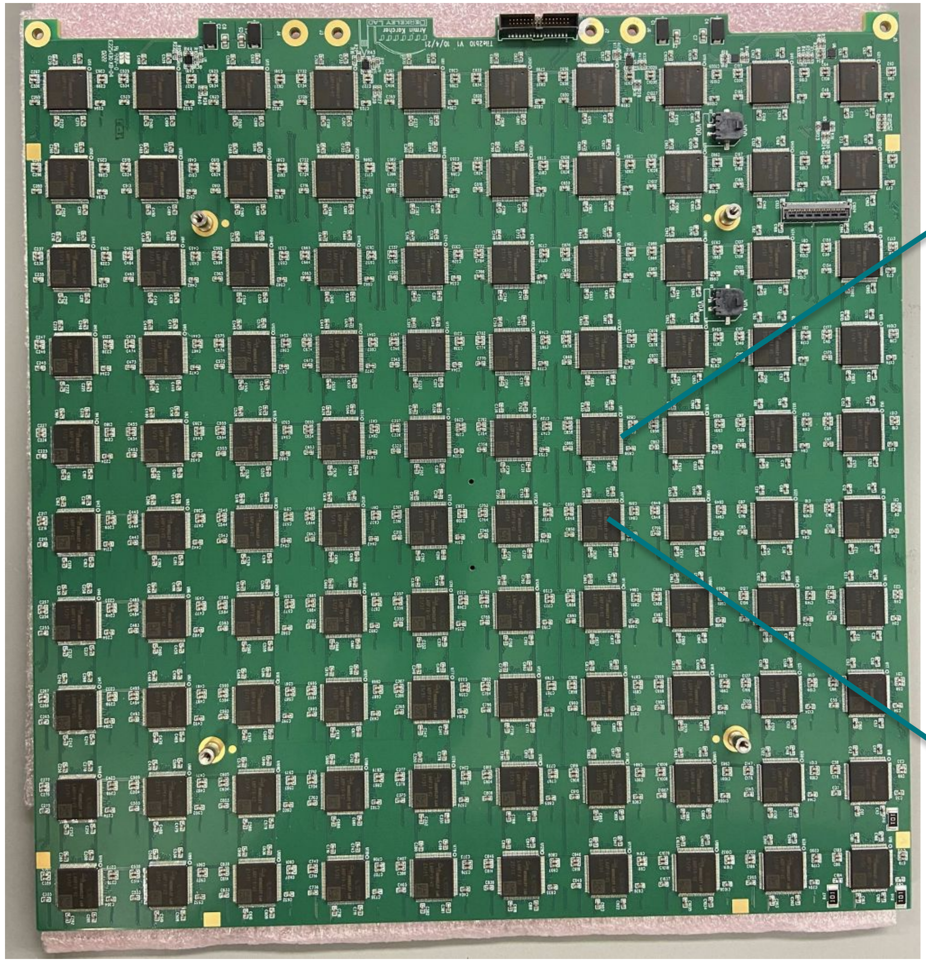
32 channels, 33 mm^2



LArPix-v2

64 channels, 25 mm^2

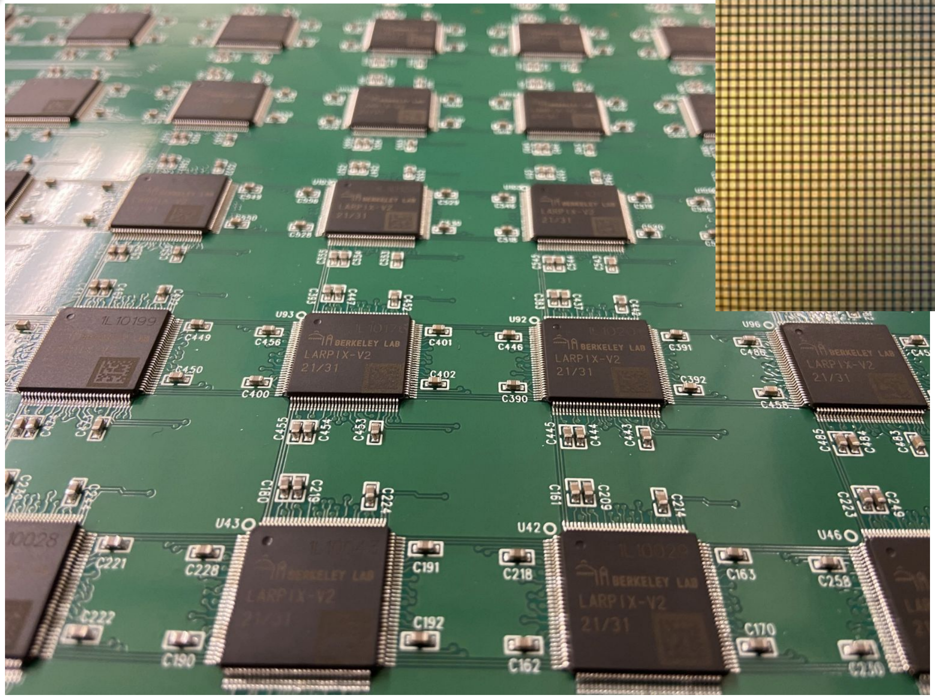
LArPix Pixel Tile

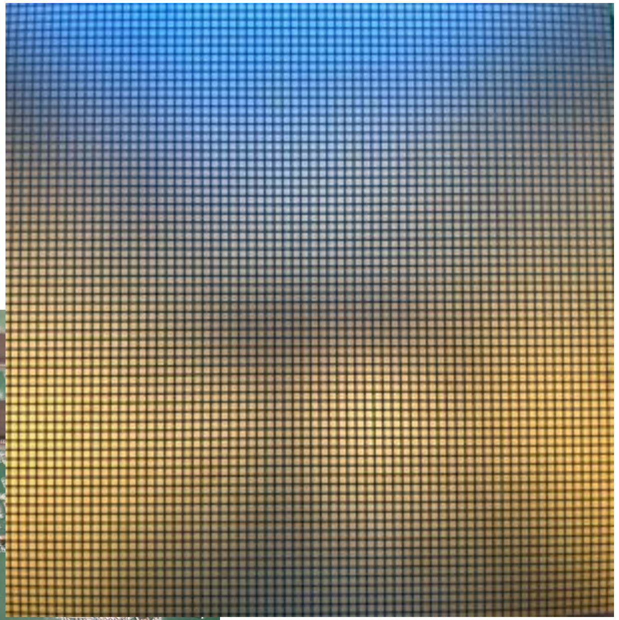


Tile with 100 LArPix-v2 ASICs (6400 channels)

Need O(10 Million) pixels for ND

Closeup of tile





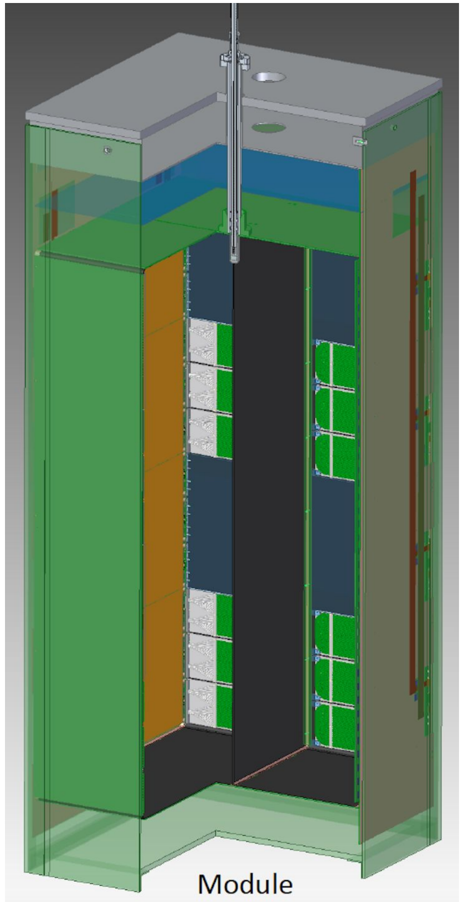
Front of tile with sensor array

Prototype tiles have 100 LArPix ASICs
(30 cm by 30 cm)
ND Tiles will scale to 160 ASICs/tile

Demonstrate system scalability in large LArTPC: ArgonCube 2x2 Demonstrator

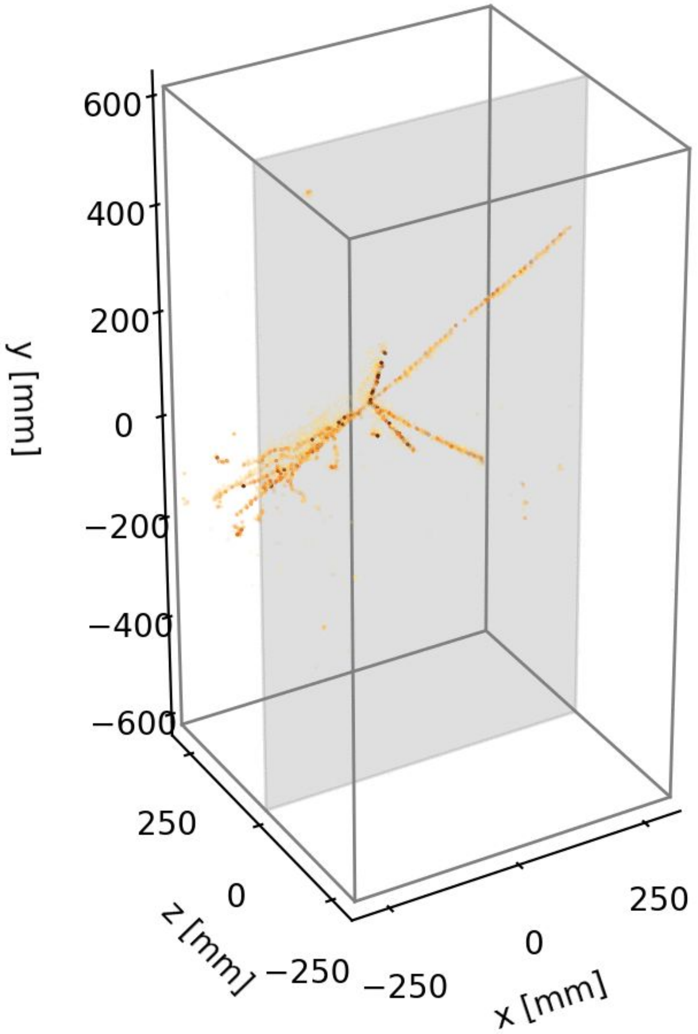
4 modular LArTPCs
Total active mass: ~3 ton
Readout area: 6.4 m^2
400k pixels, 6.3k ASICs

System successfully operated.
Demonstrator for DUNE Near Detector



ArgonCube

Demonstrate system scalability in large LArTPC: ArgonCube 2x2 Demons[illegible]

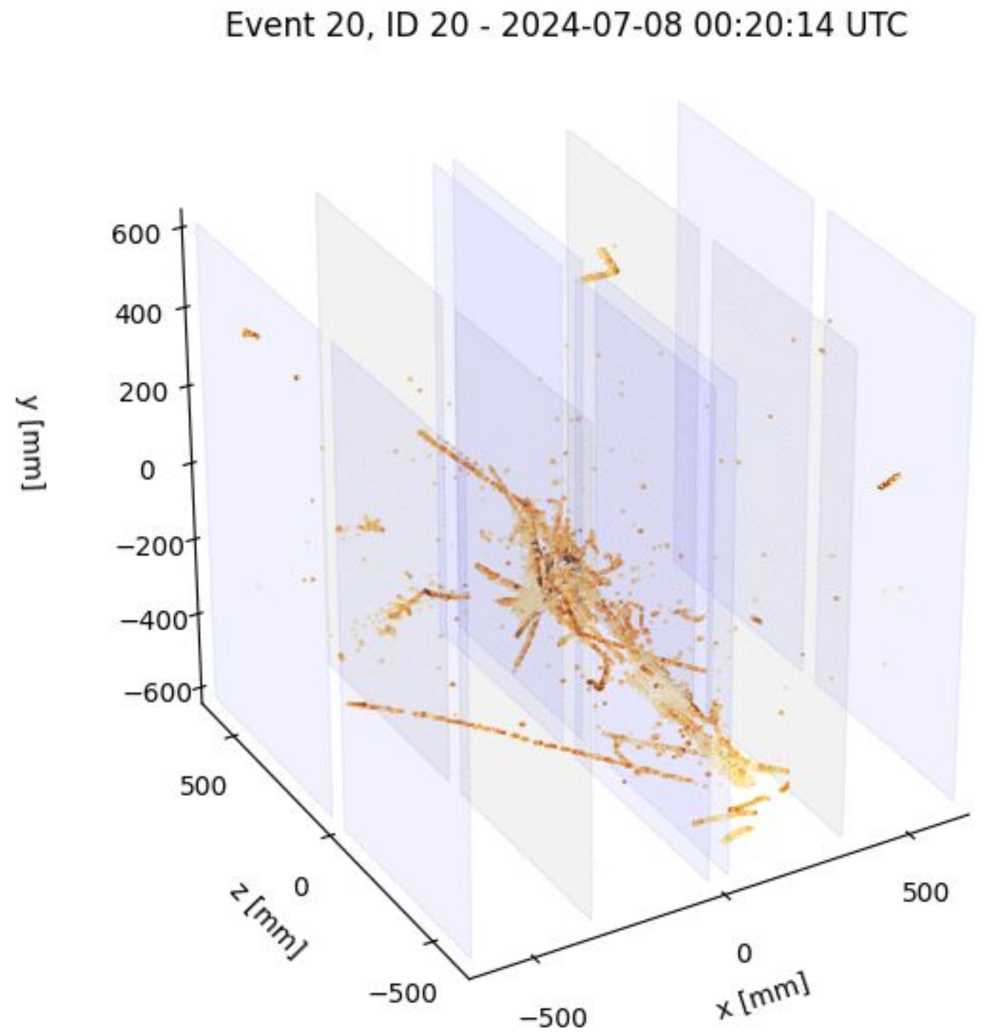


Raw data (no filtering) of cosmics in ArgonCube module0 demonstrator.

Detector delivers unprecedented track fidelity and would be impossible to implement without custom ASICs

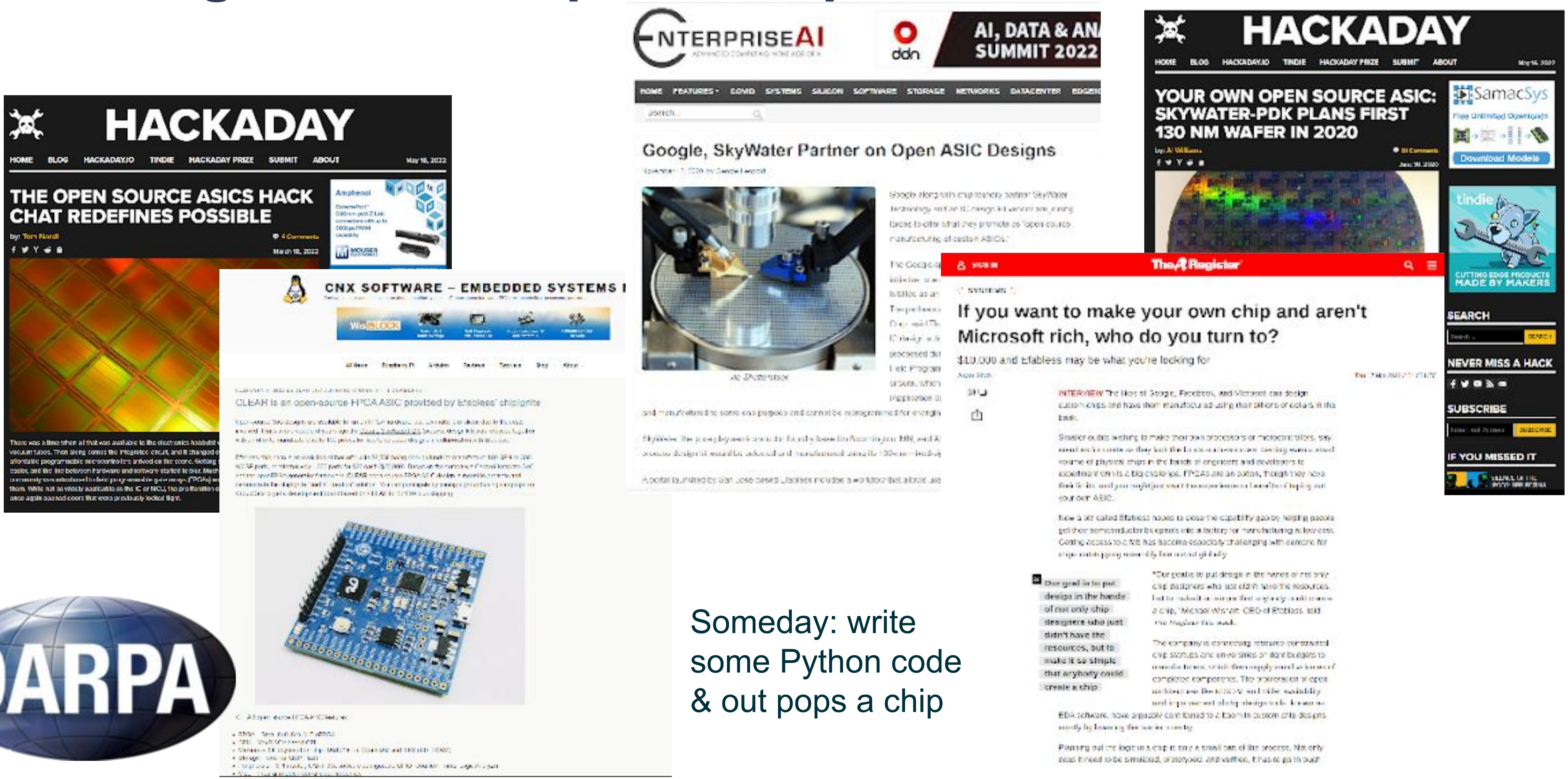
The final DUNE Near Detector will require approximately 350k ASICs to instrument a 100m^2 pixel plane (22.4 Mpix)

First Neutrino Events (DUNE ND 2X2 Demonstrator)



First-ever neutrino events measured using pixelated LArTPC at FNAL (July 7, 2024)!

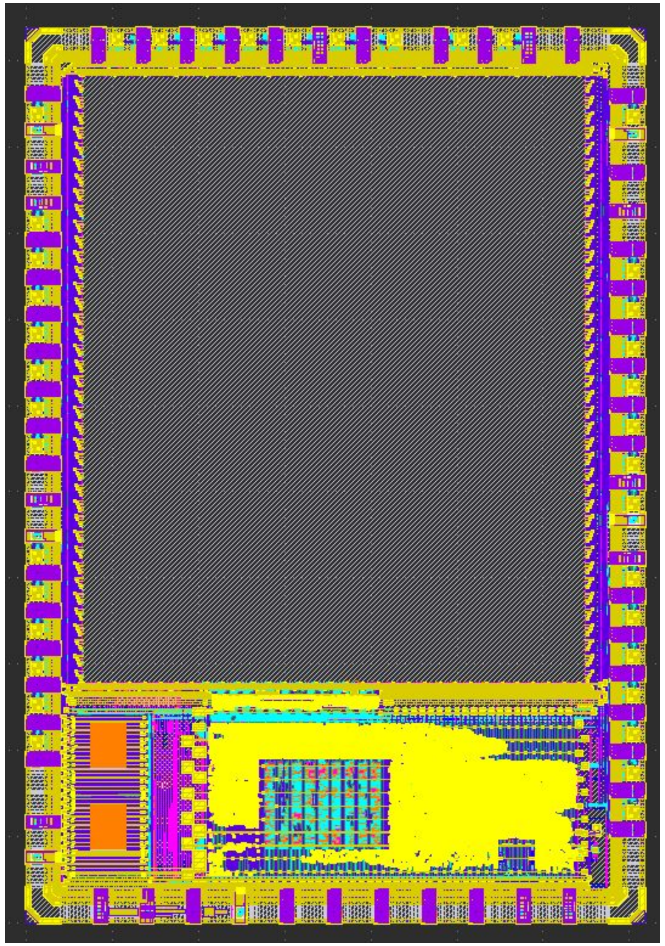
Exciting new development: Open-Source ASICs



Someday: write some Python code & out pops a chip

Open-Source design tools and Skywater 130nm PDK

All the code, no NDA, \$10k for a batch of $10mm^2$ chips, OSH Chips are free



- Venerable tools such as `magic`, `ngspice` + new additions particularly in digital synthesis and place/route
- Decent capabilities. The “harness” comes with an embedded RISC-V CPU
- The completely open PDK makes designs publishable
  - Large number of reusable designs shared on github
  - Large community of early adopters
- Google is heavily involved in pushing for Open-Source PDKs
  - Serious future AI and design automation implications

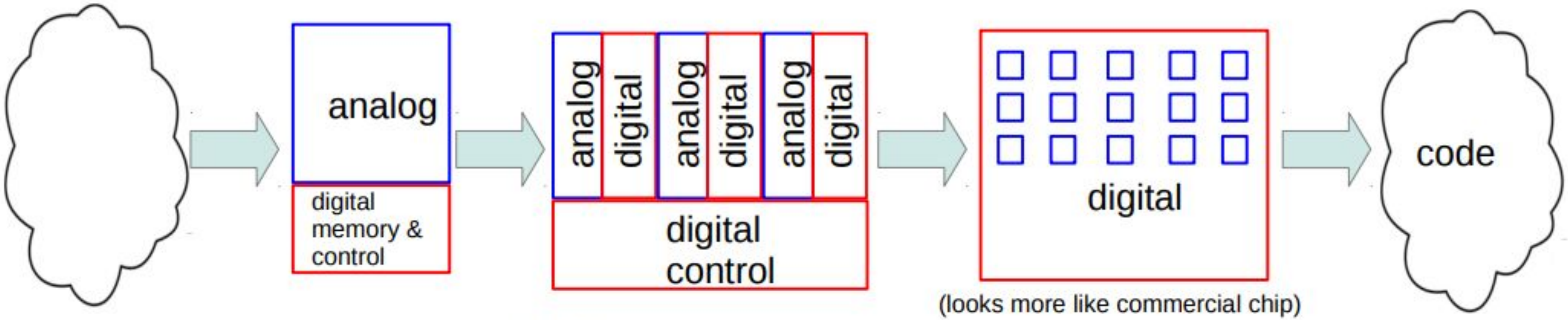
Google + skywater TECHNOLOGY

FOSS 130nm Production PDK
github.com/google/skywater-pdk

First announced in June 2020

efabless.com

Final Thought (Courtesy M. Garcia-Sciveres)



(looks more like commercial chip)

Physicist drawing transistors

Single institute team

(EEs)

FE-I4

Participating institutes:

Bonn: D. Arutinov, M. Barbero, T. Hemperek, A. Kruth, M. Karagounis.

CPPM: D. Fougeron, M. Menouni.

Genova: R. Beccherle, G. Darbo.

LBNL: S. Dube, D. Elledge, M. Garcia-Sciveres, D. Gnani, A. Mekkaoui.

Nikhef: V. Gromov, R. Kluit, J.D. Schipper

Nov. 2017 RD53 meeting, CERN

Your pic here

1980s

1990s

2000s

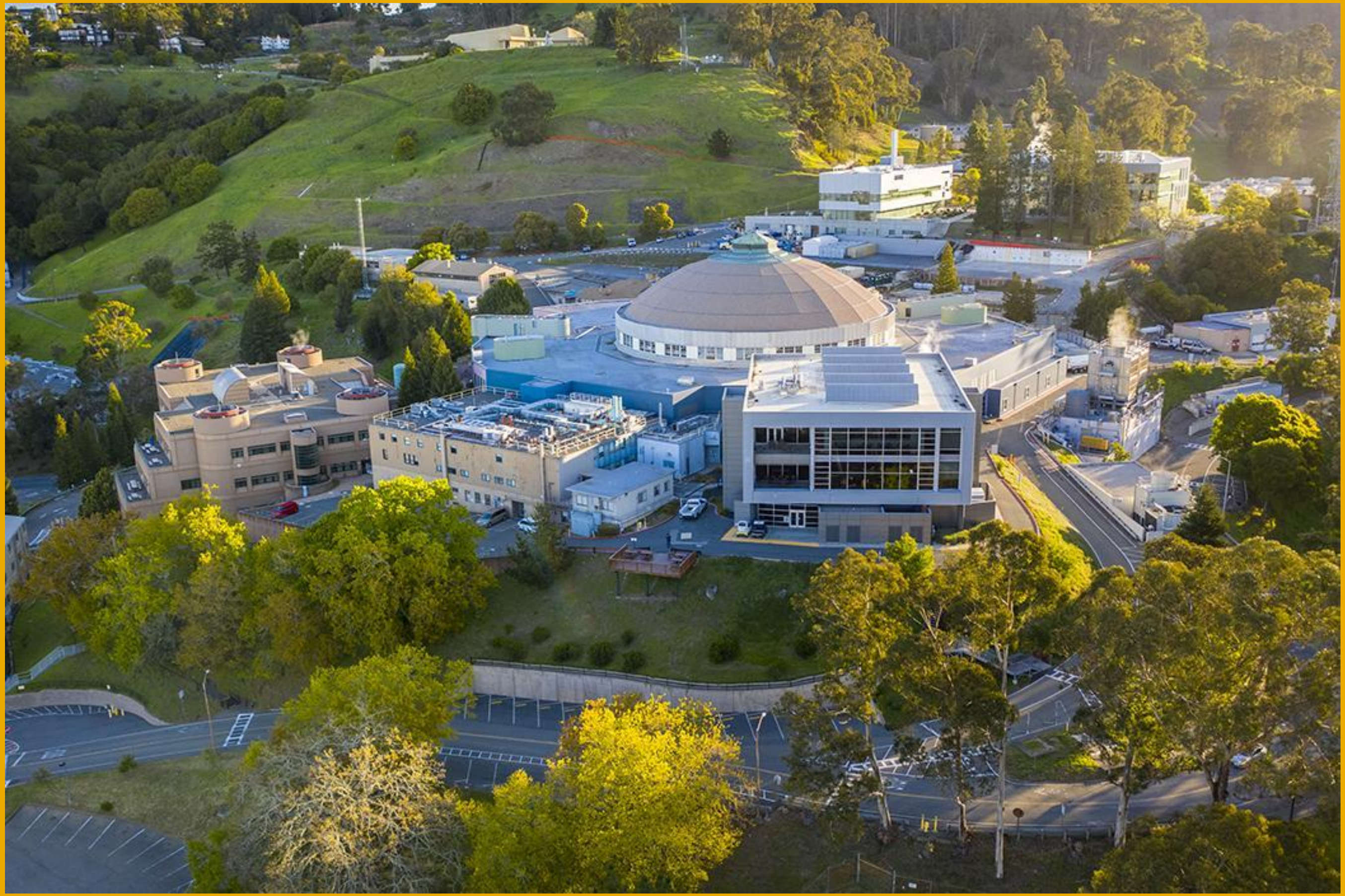
Commercial style design and validation
10^9 transistor Chips work the first time

2010s – 2020s

2030s?

M Garcia-Sciveres

Thank You



This work was supported in part by the U.S. Department of Energy under Contract No. DE-AC02-05CH11231