# HEPCAT Report

Gael Flores Avila (UCLA)

May 7, 2023

## Introduction

The Large Hadron Collider (LHC) has allowed us to experimentally test the best models for explaining the fundamental workings of the universe; the most successful of which being the standard model. This model has been extremely successful in explaining experimental data, however, there are some outstanding questions that need to be resolved. We know that the standard model is not the final answer, it is a low energy effective field theory, meaning that there must be some high energy limit at which it fails to make accurate predictions. So we carry on - testing the limits of this and other modern theories to find answers to long sought after questions.

The LHC is currently colliding protons at a center of mass energy of 13TeV and an instantaneous luminosity of $10^{34} cm^{-2} s^{-1}$. The next upgrade to the LHC will increase the luminosity to roughly 10 times the nominal, leading to a potential integrated luminosity of $4000 fb^{-1}$ over a ten year period, thus marking the beginning of the high-luminosity LHC (HL-LHC) era. [1] The UCLA group is tasked with upgrading the level 1 trigger system which is to be delivered during the long shutdown III later this decade.

## 1 Project scope

The main instrumentation goal for this project is to design, build, test, and deliver an upgrade to the level 1(L1) muon trigger digital processing board. The board, from here on referred to as kraken, will be installed at the Compact Muon Solenoid (CMS) experiment at CERN. Kraken's main purpose will be to receive muon data from various parts of the detector and run trigger algorithms to select events of interest, these data will then be passed to a high level trigger for further processing. To this end, it is necessary to learn how to design electronics through

schematics development and printed circuit board (PCB) layout, firmware development and bench testing.

## 2 Progress Report

Initial training for schematics capture was realized through the design of a smaller test board. The smaller board was designed to serve as an interface for communicating with kraken through Ethernet. The first design went through a few iterations as power calculations determined that the original design would draw more power than what was available. Integrated circuit (IC) unavailability also affected the original design, as one of the chips that we had planned on using became unavailable. After the schematic design was complete, the layout process began. Another purpose for building this small test board was to test the functionality of an Ethernet transceiver IC that would potentially be integrated into the kraken final design. The schematic was finished and reviewed by members of the group, and then the PCB layout began. The Ethernet transceiver (ET) board was completed and sent out for manufacturing after the PCB was reviewed and approved by the group. After the board and components arrived; and after some soldering difficulties in house, we had a finished version of the ET board, ready to be tested. The first step was to test the traces for shorts, and after none were found, the board was powered on. The board powered on properly and all power rails read the correct voltage levels. In testing the signal integrity, we found that signals were not propagating properly through the board, and at this point it was decided that the Ethernet transceiver IC would not be used in the final design.

### 2.1 Kraken

The design for kraken has been in the works for some time, and the schematic was mostly complete by the time I joined the CMS group at UCLA. After acquiring the aforementioned engineering skills, my next task was to aid in the design and planning for the board. The current design team consists of my Advisor, Michalis Bachtis, staff engineer, Delano Campos, and myself.

### 2.1.1 Power Supply Simulations

The large, central FPGA in kraken will operate at an core voltage of 0.8V and a current of over 300A. Due to the sensitive nature of the electronics, it is important that the power supply behaviour is well understood. The board will use a combination of linear voltage regulators and switching voltage regulators. The latter of which need to be carefully set up in order to minimize the output ripple voltage that can damage the board. Simulations using LTSpice were run on all power supplies to study the ripple voltage behaviour. This study helped in understanding the behaviour of the power supplies and some modifications to the board design were implemented.

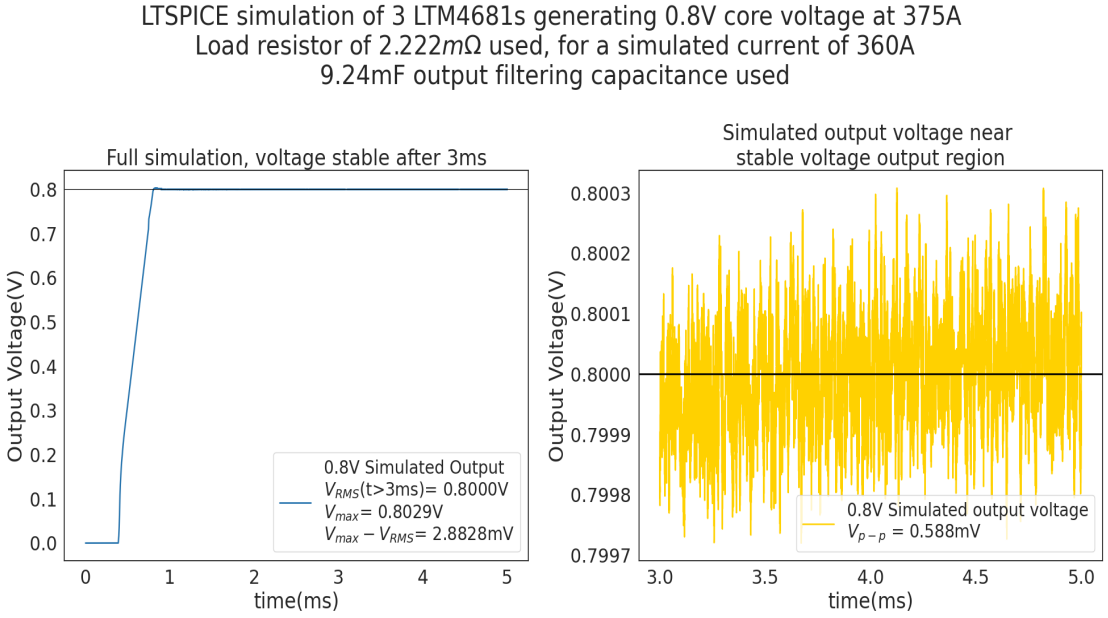


Figure 1: LTSpice simulation showing ripple voltage behaviour

### 2.1.2 Schematic Review

The schematic design of the board was carefully reviewed as a team. The design contains over 70 pages of schematics. The review was done in sections, beginning with the power supplies. This included the power supply simulations mentioned above. Each section of the review consisted of reading each component's data sheet and verifying that all devices were properly implemented. The design was discussed and changes made as necessary. Once the power supplies were validated at both the simulation and schematic levels, we reviewed all connectors and also the auxiliary FPGA that would control the peripherals of the board using an I2C interface. Next, the data transmission banks of the FPGA, along with the connectors were reviewed, and we finished with the memory chips and clock synthesizers. The review process was a big effort and significant changes to kraken were made.

### 2.1.3 PCB Layout

The layout, which is still ongoing, has been done in parallel between the design group members. Sub modules of the board are created and shared amongst ourselves. The board will be composed of 16 layers and will feature a high-density interconnect techniques such as the use of microvias and buried vias. Reduction of electromagnetic interference (EMI) will be accomplished through the use of proper routing techniques such as spacing traces properly and adding proper signal return paths.

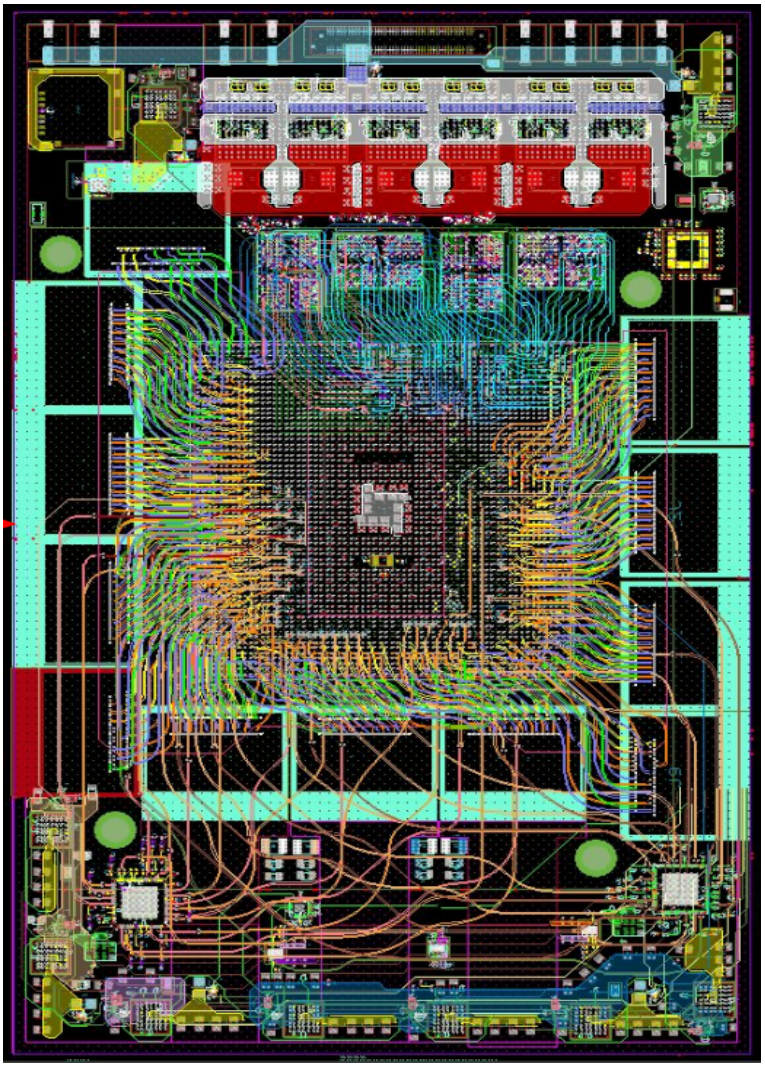

Figure 2: Current status of kraken layout

## 3 Future Work

The final PCB design is expected to be finalized by this summer. Once this is complete, the board will be sent for manufacturing and the testing, along with the programming of the firmware can begin.

## References

[1] CMS Collaboration (2020) *The Phase-2 Upgrade of the CMS level-1 Trigger* CERN-LHCC-2020-004 ; CMS-TDR-021. Available at https://cds.cern.ch/record/2714892 [Verified 28 March 2023]